Intel® IXDP425 / IXCDP1100 Development Platform

User's Guide

March 2004

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Revision History

Date	Revision	Description
March 2004	005	• Added information regarding Intel® IXP420 Network Processor variants.
June 2003	004	• Incorporated information for the Intel® IXC1100 Control Plane Processor. • Extracted BOM to a separate document. • Moved visionICE* usage to the Intel® Software Release Notes.
December 2002	003	Made minor revisions in Appendix A.
September 2002	002	Revised and updated for IXP425 software release 1.0.
July 2002	001	Initial publication for Intel IXP425 software release 1.0 Alpha.

Introduction 1

1.1 Purpose

This document details the design of the Intel® IXDP425 / IXCDP1100 Development Platform (KXIDP425BD).

The IXDP425 / IXCDP1100 platform consists of a network processor base card (BIXMB425BD) and several plug-in cards that can be plugged into the base card. The plug-in cards available are the Ethernet card (BIXD100), the ADSL card (BIXD110), and the Voltage Regulator card (BIXD120).

The base card includes the basic building blocks of the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor system. The board includes a socketed Intel® IXP425 Network Processor, SDRAM memory, boot ROM, PCI, UTOPIA-2, HSS-0, HSS-1, ENET-0 and ENET-1 plug-in slots.

Though the IXDP425 / IXCDP1100 platform is delivered with a 533-MHz IXP425 network processor, it is the development platform for *all* of the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor. Besides the IXP425 network processor, the Intel® IXP4XX Product Line includes the IXP420, IXP421, and IXP422 network processors.

Additionally, a connector is supplied for the base-card power supply. The Ethernet cards are connected (plugged in) to the base card via the Ethernet connectors. The ADSL card is connected to the base card via the UTOPIA-2 connector. The Voltage Regulator card will be connected to the base card via the Voltage Regulator connector. The base card and cards are available as a package named "Intel® IXDP425 / IXCDP1100 Development Platform."

1.2 Intended Audience

The intended audience of this document are hardware architects and developers that are developing the hardware of applications based on the IXP4XX Product Line Network Processor or the IXC1100 Control Plane Processor. Typical applications include residential gateways, SOHO and home routers, network printers, control plane, integrated access devices (IAD), wireless LAN access-point customer-premises equipment, mini DSLAMs, industrial controllers, high-performance cable and DSL modems, Ethernet switches, and hot-spot wireless LAN access equipment.

It is expected that the reader has obtained the documents listed in "Related Documents" on page 8 and is able to make references to them when necessary. This document does not explore the internal architecture of the IXP4XX Product Line Network Processor or the IXC1100 Control Plane Processor, but will touch on the processor's interfaces to peripherals that are used on the IXDP425 / IXCDP1100 platform. Sheet numbers of the listed schematics will be referenced in parenthesis, when interfaces are being explained in this document. The schematics are available on the Documentation CD that shipped with the IXDP425 / IXCDP1100 platform or through your local Intel representative.

1.3 High-Level Design Principles

The IXDP425 / IXCDP1100 platform is a flexible development platform package that is designed to:

- Demonstrate the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor's capabilities in aspects of performance, functionality, and hardware and software architectural superiority
- Enable customers to use the Intel® IXP4XX Product Line and IXC1100 Control Plane Processor Software Development Kit software to develop applications targeted for the IXP4XX Product Line Network Processor or the IXC1100 Control Plane Processor.

A modular approach is used for all important interfaces so that cards can quickly be developed to allow customers to implement and debug their applications without the worry of debugging processor-related issues. This modular approach allows customers to quickly prototype the final platform to allow the software design team to complete design on a final platform identical to the final product.

1.4 Related Documents

Title	Document Number
Intel® IXDP425 / IXCDP1100 Development Platform Quick Start Guide	253177
Intel® IXPD425 / IXCDP1100 Platform Boot-Loader Flash Conversion Guide	253201
Intel® IXP4XX Product Line and IXC1100 Control Plane Processor Hardware Design Guidelines	252817
Intel XScale ® Core Developer's Manual	273473
Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Datasheet	252479
Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Developer's Manual	252480
Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processors Specification Update	252702
Intel® IXP400 Software Programmer's Guide	252539
3-Volt Intel StrataFlash® Memory 28F128J3A (x8/x16) Datasheet	290667
3-Volt Intel StrataFlash® Memory 28F128J3A (x8/x16) Specification Update	298130
Intel®LXT972A 3.3V Dual-Speed Fast Ethernet Transceiver Datasheet	249186
LXT971A/972A PHY Transceivers Specification Update	249354
BIXMB425BD *Base Card Schematics and Bill of Materials*	
BIXD100 Ethernet Card Schematics and Bill of Materials	
BIXD110 ADSL Card Schematics and Bill of Materials	
BIXD120 Voltage Regulator Card Schematics and Bill of Materials	

1.5 Acronyms

ADSL	Asymmetric Digital Subscriber Line
AAL	ATM Adaptation Layers
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
API	Application Program Interface
Assert	The logically active value of a signal or bit.
ATM	Asynchronous Transfer Mode
ATM-TC	Asynchronous Transmission Mode – Transmission Convergence
BTB	Branch Target Buffer
Clean	An operation that updates external memory with the contents of the specified line in the data/mini-data cache if any of the dirty bits are set and the line is valid. There are two dirty bits associated with each line in the cache so only the portion that is dirty will get written back to external memory. After this operation, the line is still valid and both dirty bits are deasserted.
Coalescing	Bringing together a new store operation with an existing store operation already resident in the write buffer. The new store is placed in the same write buffer entry as an existing store when the address of the new store falls in the four-word, aligned address of the existing entry. This includes, in PCI terminology, write merging, write collapsing, and write combining.
CPE	Customer Premise Equipment
CRC	Cyclical Redundancy Check
DDR	Double-Data Rate
Deassert	The logically inactive value of a signal or bit.
DIA	Development Investment Approval
DiffServ	Differentiated Services
DMA	Direct Memory Access
DSL	Digital Subscriber Line
DSP	Digital Signal Processor
E1	Euro 1 trunk line
FCS	Frame-Check Sequence
FIFO	First In First Out
Flush	An operation that invalidates the location(s) in the cache by deasserting the valid bit. Individual entries (lines) may be flushed or the entire cache may be flushed with one command. Once an entry is flushed in the cache it can no longer be used by the program.
FRAD	Frame Relay Access Device

FRF	Frame Relay Forum
FXO	Foreign Exchange Office
FXS	Foreign Exchange Subscriber
G.SHDSL	ITU G series specification for symmetric High-Bit-Rate, Digital Subscriber Line
GCI	General Connection Interface
GE	Gigabit Ethernet
GPIO	General-Purpose Input/Output
HDLC	High-Level Data Link Control
HDSL	High-Bit-Rate Digital Subscriber Line
HDSL2	High-Bit-Rate, Digital Subscriber Line, Version 2
HEC	Head-Error Correction
HPI	Host-Port Interface
HPNA	Home-Phone Network Alliance
HSS	High-Speed Serial (port)
HSSI	High-Speed, Serial Interface
IAD	Integrated Access Device
IBC	Integrated Business Communications
IKE	Internet Key Exchange
IMA	Inverse Multiplexing over ATM
IOM	ISDN Orientated Modular
IP	Internet Protocol
IPsec	Internet Protocol Security
ISDN	Integrated Services Digital Network
IXA	Internet Exchange Architecture
IXP	Internet Exchange Processor
LAN	Local Area Network
LFSR	Linear Feedback Shift Register
LSb	Least-Significant bit
LSB	Least-Significant Byte
LUT	Look-Up Table
MAC	Media Access Controller
MDIO	Management Data Input/Output
MIB	Management Information Base
MII	Media-Independent Interface
MLPPP	Multi-Link, Point-to-Point Protocol

MMU	Memory Management Unit
MRD	Marketing Requirements Document
MSb	Most-Significant bit
MSB	Most-Significant Byte
MVIP	Multi-Vendor Integration Protocol
MVIP	Multi-Vendor Integration Protocol
NPE	Network Processor Engine
NRZI	Non-Return To Zero Inverted
OC-3	Optical Carrier Class 3 (155.52 Mbps)
PBX	Private Branch Exchange
PCI	Peripheral Component Interface
PEC	Programmable Event Counters
PHY	Physical Layer (Layer 1) Interface
PRD	Product Requirements Document
Reserved	A field that may be used by an implementation. Software should not modify reserved fields or depend on any values in reserved fields.
RMII	Reduced Media Independent Interface
RX	Receive (HSS is receiving from off-chip)
SA2	Intel® StrongArm* II (now referred to as Intel XScale® Core)
SAR	Segmentation and Reassembly
SAS	Systems Architecture Specification
SDRAM	Synchronous Dynamic Random Access Memory
SDSL	Symmetrical Digital Subscriber Line
SFD	Start of Frame Delimiter
SIP	Session Initiation Protocol
SNMP	Simple Network Management Protocol
SOHO	Small Office Home Office
T1	Type 1 trunk line
TDM	Time Division Multiplex
TLB	Translation Look-Aside Buffer
ToS	Type of Service
TX	Transmit (HSS is transmitting off-chip)
UART	Universal Asynchronous Receiver-Transmitter
UTOPIA	Universal Test and Operation PHY Interface for ATM
VDSL	Very-High-Speed, Digital Subscriber Line

VoDSL	Voice-Over-Digital Subscriber Line
VoFR	Voice Over Frame Relay
VoIP	Voice-Over-Internet Protocol
VPN	Virtual Private Network
WAN	Wide-Area Network
xDSL	Any Digital Subscriber Line

1.6 Naming Conventions

The following conventions are used to identify and classify signal names:

- '_N' after a name indicates that the signal is active low:
- 'I' indicates the pin is input-only.
- 'O' indicates the pin is output-only.
- 'I/O' indicates the pin is bidirectional
- 'Z' indicates tri-state.
- 'TTL' indicates transistor-transistor logic.
- Indicates open drain pin.
- 'U'/'D' indicates pull-up/pull-down resistor.
- Suffix 'h' indicates Hexadecimal values (example: 2F_8000h).
- Suffix 'b' indicates Binary values (example: 010110b).
- _DNP indicates "Do not populate" this component, if this designation is found on the schematics.
- GND_DIGITAL indicates digital ground plane for the base card I/O card.
- TP indicates Test Points.

Intel® IXDP425 / IXCDP1100 Development Platform Overview 2

The IXDP425 / IXCDP1100 platform consists of:

- BIXMB425BD Base Card
- Two BIXD100 Ethernet Cards
- One BIXD110 ADSL CPE Card
- One BIXD120 Voltage Regulator Card

All of the BIXD1x0 Cards plug into the BIXMB425BD base card.

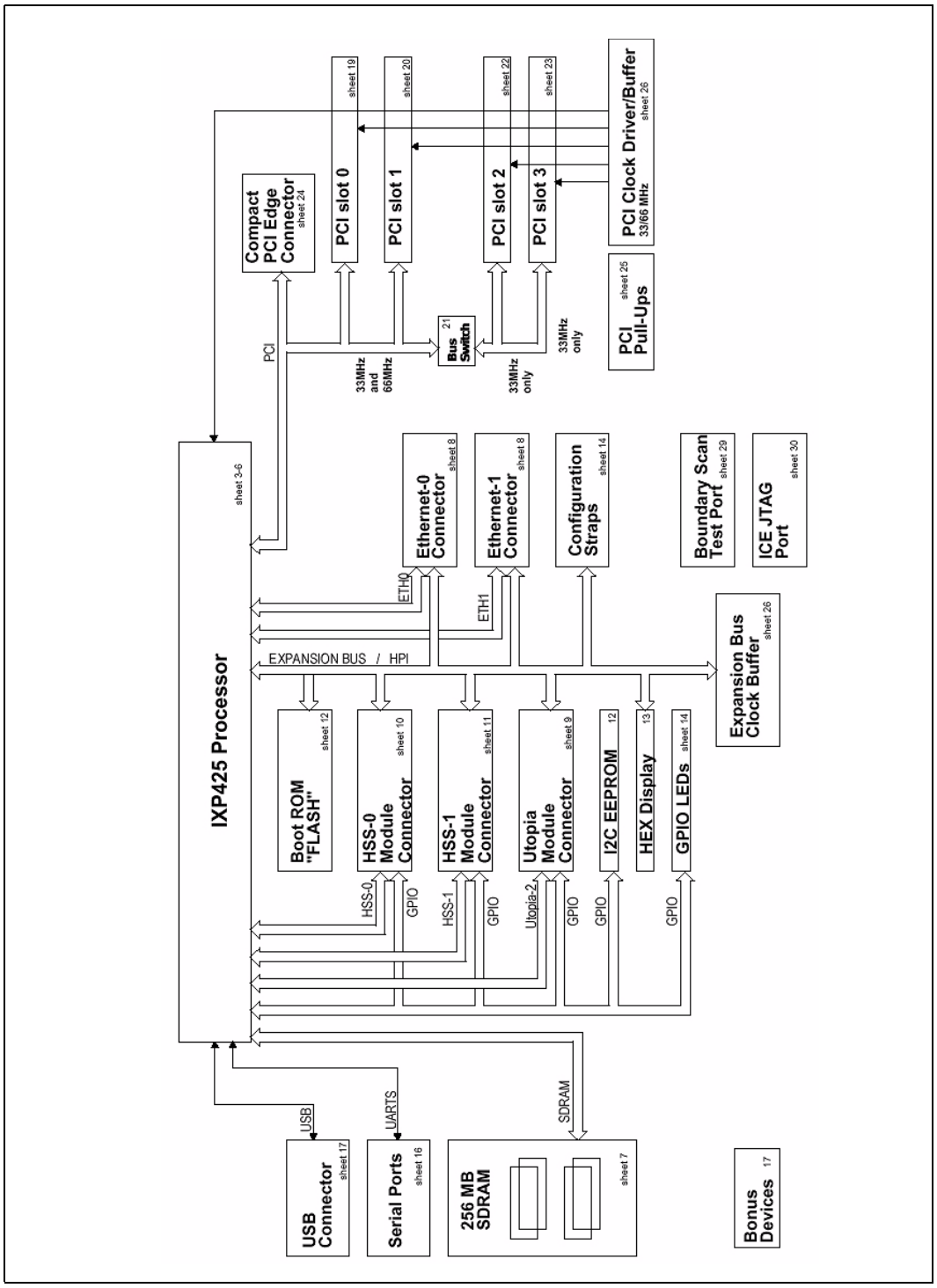
2.1 BIXMB425BD Network Processor Base Card

The BIXMB425BD base card consists of:

- IXP425 network processor
- Two UART ports (1 High-Speed, 1 Console)
- Four PCI slots
- Flash memory (Boot ROM)
- HSS-0 card connector
- HSS-1 card connector
- I^2C EEPROM
- UTOPIA-2 card connector
- SDRAM (256 Mbyte)
- ENET-0 card connector
- ENET-1 card connector
- Voltage Regulator card connector

The connections between the devices and connectors on the base card are shown in Figure 1 along with its sheet number in the BIXMB425BD base card schematics. Details on each device are described in the next chapter.

Figure 1. BIXMB425BD Base Card Block Diagram



2.2 KXIDP425BD Components on the BIXMB425BD Base Card

Figure 2. Components on the BIXMB425BD Base Card — Top View

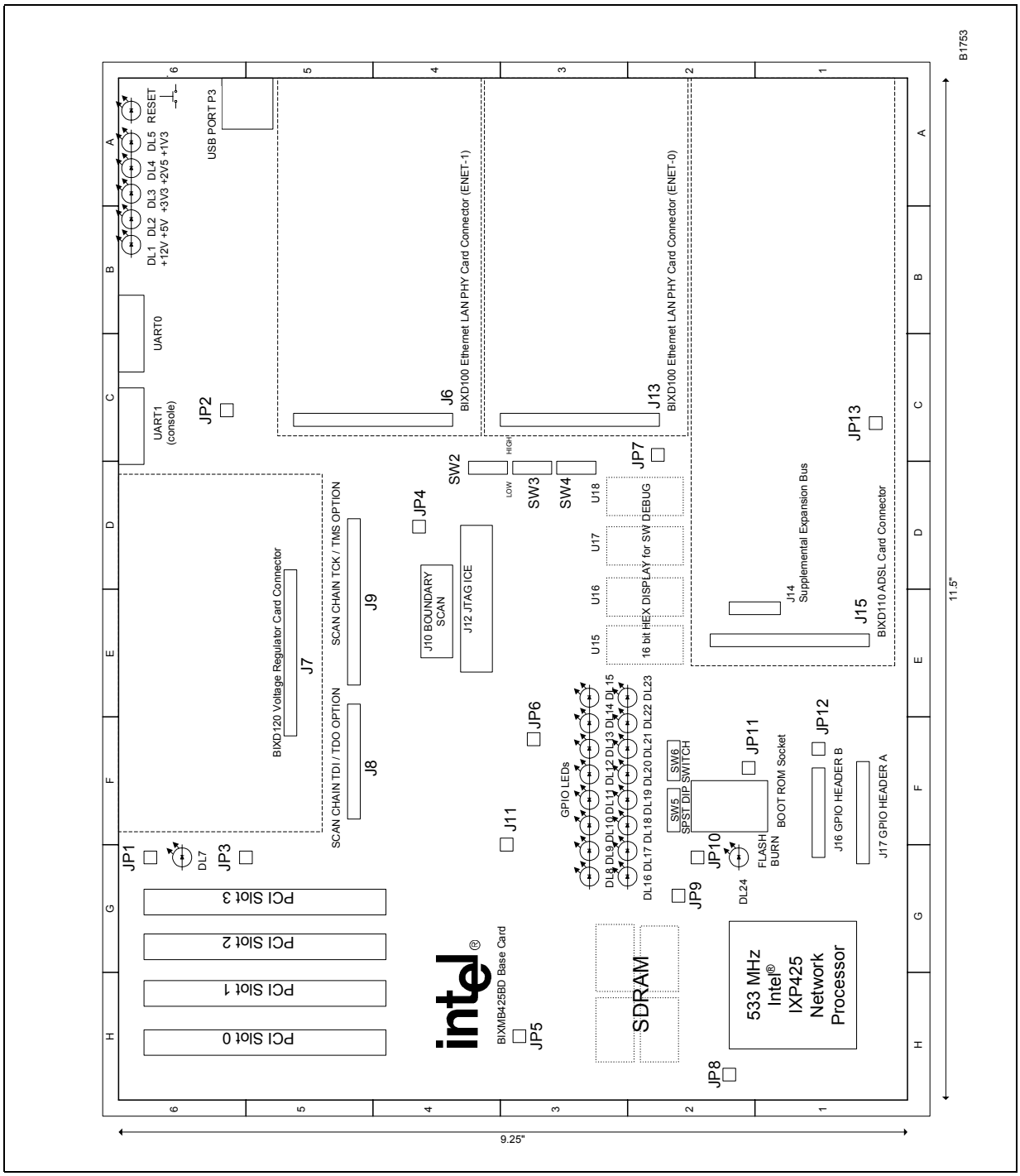
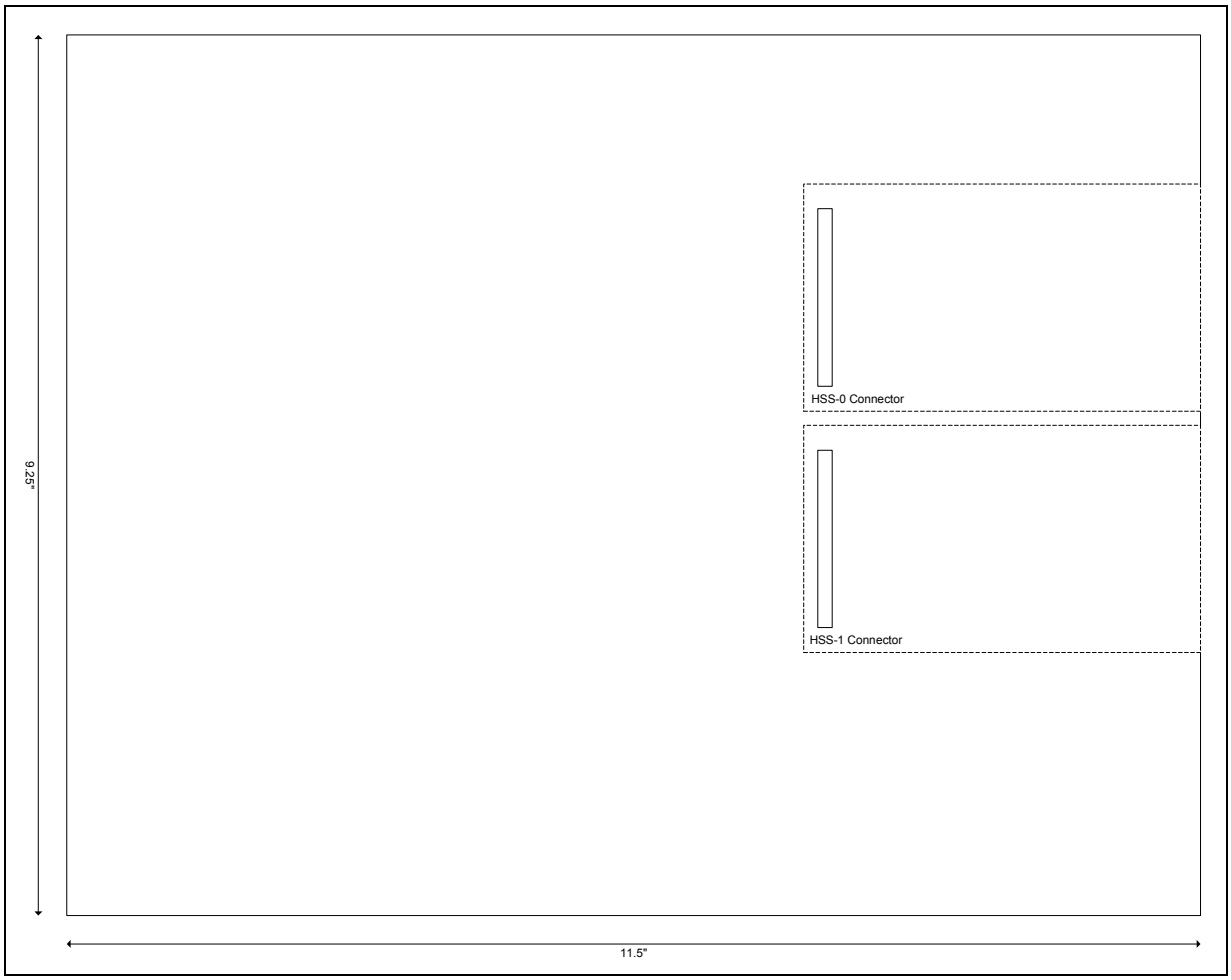


Figure 2 and Figure 3 show the IXDP425 / IXCDP1100 platform's components-placement diagram on the BIXMB425BD base card (top and bottom view). Also shown are the locations of jumpers, headers, connectors, and LEDs used in the design. For more information on the bill of materials of the BIXMB425BD Base card see the BIXMB425BD *Base Card Schematics and Bill of Materials* which are included on the Documentation CD that ships with the platform or available by contacting your local Intel representative.

Note: J6 and J13, are connected to the BIXD100 Ethernet Cards. J15 is connected to the BIXD110 ADSL Card. J7 is connected to the BIXD120 Voltage Regulator Card.

Note: The HSS-0 and HSS-1 Connectors in Figure 3 have no cards attached

Figure 3. Components on the BIXMB425BD Base Card — Bottom View



For reference, Table 1 lists the jumpers and Table 2 lists the connectors and headers that are shown in Figure 2 and each provides a brief description of each component and its default setting. These components are described in more detail in the following chapters.

Table 1. Jumper Setting Descriptions for the Intel® BIXMB425BD Base Card

Reference	Description	Default Setting
JP1	GND	NO SHUNT
JP2	GND	NO SHUNT
JP3	PCI Clock – Allow 66 MHz operation through the PCI slot. (1-2) Run at 33 MHz on the PCI slot (2-3)	SHUNT 1-2
JP4	GND	NO SHUNT
JP5	GND	NO SHUNT
JP6	Expansion bus clock – 33 MHz external oscillator (1-2) or GPIO15 (2-3)	SHUNT 1-2
JP7	GND	NO SHUNT
JP8	cPCI Clock – Allow 66 MHz operation through the compact PCI slot. (1-2) Run at 33 MHz on the compact PCI slot (2-3)	NO SHUNT
JP9	+3.3 V Power Measurement	NO SHUNT
JP10	GND	NO SHUNT
JP11	Flash Boot Address – 0000 0000h (1-2) 0080 0000h (2-3)	SHUNT 1-2
JP12	UTOPIA-2 input and output clock – 33 MHz Enabled: (1-2), Disabled (2-3)	SHUNT 1-2
JP13	+1.3 V Power Measurement	NO SHUNT

Table 2. Connector/Header Descriptions for the Intel® BIXMB425BD Base Card (Sheet 1 of 2)

Reference	Description	Default (factory) Setting
J1	UART pins access (unpopulated)	NO SHUNT
J2	PCI Slot	NO SHUNT
J3	PCI Slot	NO SHUNT
J4	PCI Slot	NO SHUNT
J5	PCI Slot	NO SHUNT
J6	ENET-1 Connector	NO SHUNT
J7	Voltage Regulator Card Connector	NO SHUNT
J8	Boundary Scan Chain (TDI/TDO)	SHUNT 1-2, 3-4
J9	Boundary Scan Chain (TCK/TMS)	1-2,3-4,5-6,7-8,9-10,11-12,13-14,15-16,17-18,19-20, 21-22,23-24,25-26,27-28, 29-30,31-32,33-34,35-36, 37-38,39-40,41-42,43-44
J10	Boundary Scan Connector	NO SHUNT

Table 2. Connector/Header Descriptions for the Intel® BIXMB425BD Base Card (Sheet 2 of 2)

Reference	Description	Default (factory) Setting
J11	PCI Clock – GPIO (1-2) 33 MHz external oscillator (3-4) 66 MHz external oscillator (5-6)	SHUNT 3-4
J12	ICE Emulator Connector	NO SHUNT
J13	ENET-0 Connector	NO SHUNT
J14	Utopia-2 Extender Connector	NO SHUNT
J15	Utopia-2 Connector	NO SHUNT
J16	GPIO Header B	NO SHUNT
J17	GPIO Header A	SHUNT 1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, 15-16, 17-18, 19-20, 21-22, 23-24, 25-26, 27-28, 29-30, 31-32
J18	HSS-0 Connector	NO SHUNT
J19	HSS-1 Connector	NO SHUNT
J20	cPCI Connector (unpopulated)	NO SHUNT

BIXMB425BD Base Card Hardware Design Description 3

3.1 Processor

The Intel® IXP425 Network Processor can operate at clock speeds of 266 MHz, 400 MHz, and 533 MHz and is available in Commercial Temperature and Extended Temperature. The 533 MHz IXP425 network processor is used on the IXDP425 / IXCDP1100 platform base card, but the platform is compatible with — and is the development platform for — all of the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor. (Besides the IXP425 network processor, the IXP4XX product line includes the IXP420, IXP421, and IXP422 network processors.)

An external 33.333 MHz oscillator acts as the input clock signal at OSC_IN of the IXP425 network processor. A 33.33 MHz crystal can also be used to clock the IXP425 network processor as a cheaper alternative to an oscillator. The crystal should be connected between OSC_IN and OSC_OUT of the IXP425 network processor. If the IXP425 network processor is required to operate at speeds lower than 533 MHz, the configuration strapping for the Intel XScale core clock can be set accordingly to allow slower clock speeds, i.e., 266 MHz or 400 MHz (see "Configuration Straps" on page 29).

The features of the Intel® IXP425 Network Processor are summarized below. The IXDP425 / IXCDP1100 platform is designed to take full advantage of these features.

- Intel XScale core running at ratios of x2, x3, and x4 the system clock rate of 133 MHz
- Three NPEs for layer 2 packet/frame network processing
- Two 10/100 Full duplex IEEE802.3 MAC with two (2) MII interfaces
- Dedicated SDRAM 32-bit data memory interface operating at 133 MHz (equal to system clock frequency). Supports up to two physical banks, each bank up to two chips, of 64 Mb, 128 Mb, 256 Mb and 512 Mb memory configuration, 2- and 3-cycle CAS latency. 13-bit address. Maximum: 256 MB. Minimum: 8 MB.
- Expansion Bus: 24-bit address, 16-bit data, eight chip selects, Glueless interface to Intel flash, Motorola addressing mode, Intel addressing-mode peripherals.
- HPI bus (pins shared with Expansion Bus): compliant with Texas Instruments HPI, HPI-8, HPI-16 bus Host Peripheral Interface protocols
- UTOPIA-2 interface, 8-bit data path
- Two High-Speed Serial TDM buses. HSS-0 and HSS-1
- Two UARTS: one High-Speed (921Kbaud) used for supporting fast UART device; one Console (921Kbaud) used for VxWorks* or Linux* console monitoring
- PCI ver2.2 bus: 32-bit Address/Data bus. 33 or 66 MHz operation. Built-in arbiter supports up to four external bus masters
- 16 GPIOs
- USB 1.1 Device Controller supporting full-speed USB Version 1.1 data rate

More information about the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor is available in the *Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Datasheet* and the *Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Developer's Manual*.

3.2 Memory Map

The Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor implement a single address map that is used for all internal memory and register space. The complete address space consists of 2^32 byte addressable locations.

Table 3. Memory Map (Sheet 1 of 2)

Start Address	End Address	Size	Use
0000_0000	0FFF_FFFF	256 MB	Expansion Bus Data†
0000_0000	3FFF_FFFF	1 GB	SDRAM Data†
4000_0000	47FF_FFFF	128 MB	Reserved
4800_0000	4FFF_FFFF	128 MB	PCI Data
5000_0000	5FFF_FFFF	256 MB	Expansion Bus Data
6000_0000	63FF_FFFF	64 MB	Queue manager
6400_0000	BFFF_FFFF		Reserved
C000_0000	C3FF_FFFF	64 MB	PCI Controller Configuration and Status Registers
C400_0000	C7FF_FFFF	64 MB	Expansion Bus Configuration Registers
C800_0000	C800_0FFF	1 KB	High-Speed UART
C800_1000	C800_1FFF	1 KB	Console UART
C800_2000	C800_2FFF	1 KB	Internal Bus Performance Monitoring Unit
C800_3000	C800_3FFF	1 KB	Interrupt Controller
C800_4000	C800_4FFF	1 KB	GPIO Controller
C800_5000	C800_5FFF	1 KB	Timers
C800_6000	C800_6FFF	1 KB	WAN/HSS NPE – Not User Programmable
C800_7000	C800_7FFF	1 KB	Ethernet NPE A – Not User Programmable
C800_8000	C800_8FFF	1 KB	Ethernet NPE B – Not User Programmable
C800_9000	C800_9FFF	1 KB	Ethernet MAC A

† The lowest 256 MB of address space is configurable based on the value of a configuration register located in the Expansion Bus Controller.

- When the configuration register is set to logic 1, the Expansion Bus occupies the lowest 256 MB of address space.
- When the configuration register is set to logic 0 the SDRAM occupies the lowest 256 MB of address.

  In both cases, the SDRAM occupies the 768 MB immediately following the lowest 256 MB and the Expansion Bus can be accessed starting at address 5000_0000.

  The largest SDRAM memory size supported by the IXDP425 / IXCDP1100 platform is 256 MB. The actual memory implemented in any given configuration will be aliased (repeated) to fill the 1 GB SDRAM address space. Due to aliasing, all of the SDRAM will be accessible even when the Expansion Bus occupies the lowest 256 MB of address space. On reset, the configuration register in the Expansion Bus will be set to logic 1. This setting is required because the dedicated boot memory is flash memory located on the Expansion Bus.

Table 3. Memory Map (Sheet 2 of 2)

Start Address	End Address	Size	Use
C800_A000	C800_AFFF	1 KB	Ethernet MAC B
C800_B000	C800_BFFF	1 KB	USB Controller
C800_C000	C800_FFFF		Reserved
C801_0000	CBFF_FFFF		Reserved
CC00_0000	CC00_00FF	256 Byte	SDRAM Configuration Registers
CC00_0100	FFFF_FFFF		Reserved

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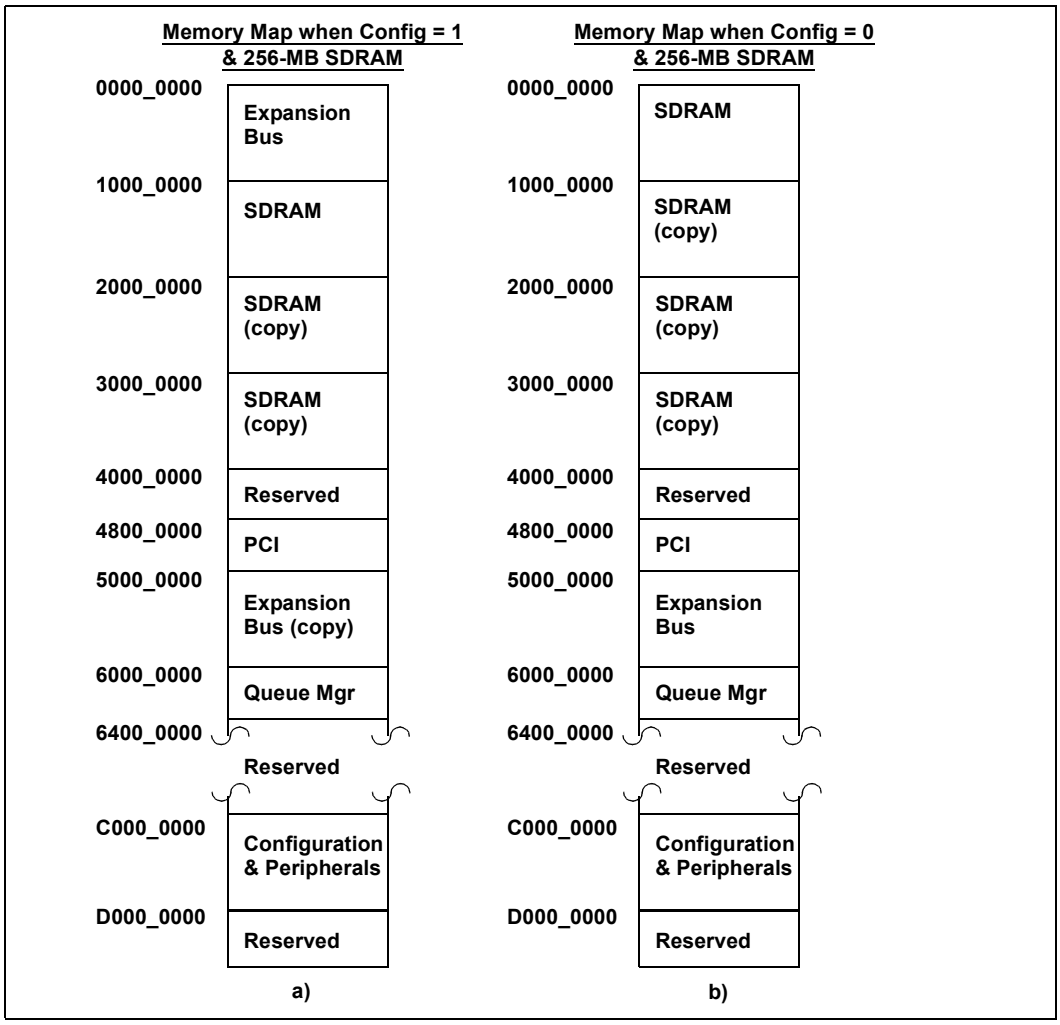
Figure 4. BIXMB425BD Memory Map and Configuration Register Setting



3.3 SDRAM Memory

The Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor support PC-133 compatible SDRAM. The banks are accessed 32 bits at a time. The maximum configuration is two physical SDRAM devices per each bank, each using two independent chip selects. A maximum of 256 Mbyte of SDRAM can be connected. The minimum SDRAM size supported is 8 Mbyte using one chip. Table 4 lists some supported memory configurations. The Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor are designed to support the full range of SDRAM memory from 8 Mbyte through 256 Mbyte.

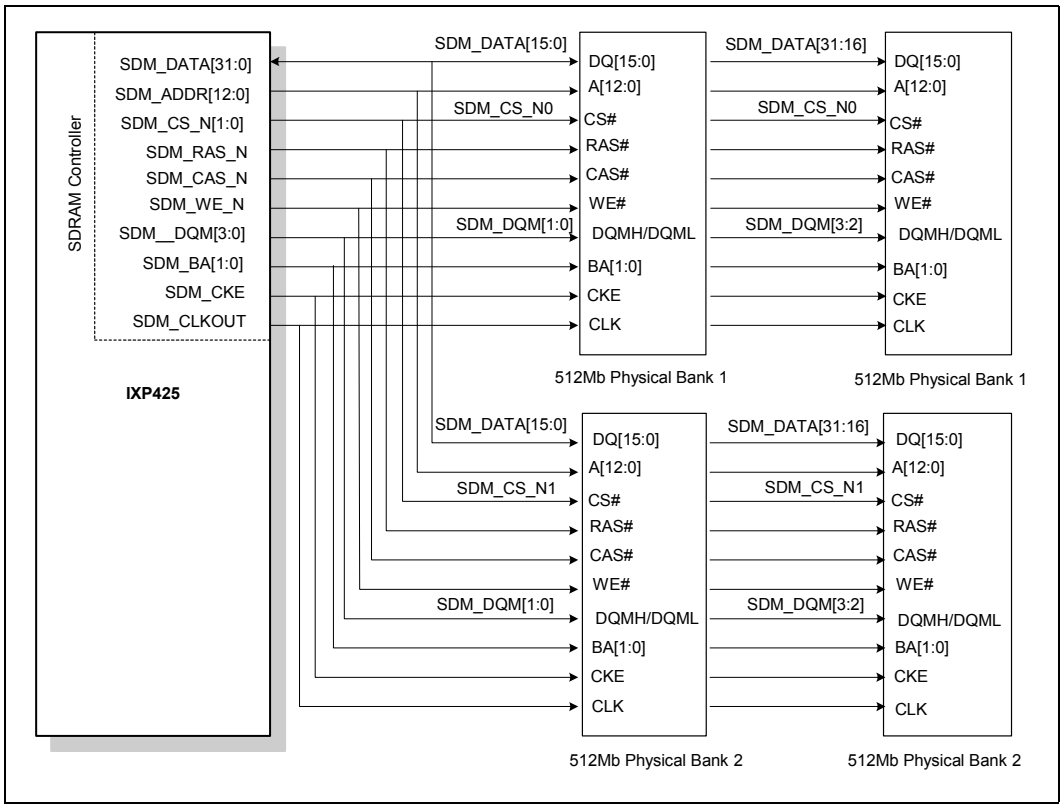
Table 4. Supported Memory Configurations

SDRAM Tech.	SDRAM Type	# Chips	Address Size		Total Mem. Size
			Row	Column	
64 Mbit	2 M x32	1	11	8	8 Mbyte
		2	11	8	16 Mbyte
64 Mbit	4 M x16	2	12	8	16 Mbyte
		4	12	8	32 Mbyte
128 Mbit	8 M x16	2	12	9	32 Mbyte
		4	12	9	64 Mbyte
256 Mbit	16 M x16	2	13	9	64 Mbyte
		4	13	9	128 Mbyte
512 Mbit	32 M x16	2	13	10	128 Mbyte
		4	13	10	256 Mbyte

The 256-Mbyte, dual physical bank, 512-Mbit, four-chip 32M-x-16 memory configuration is implemented in the KIXDP425BD Development Platform (Sheet 7). All chips are powered with +3.3 V (+3V3) power supply, clocked at 133 MHz by the IXP425 network processor's SDM_CLKOUT.

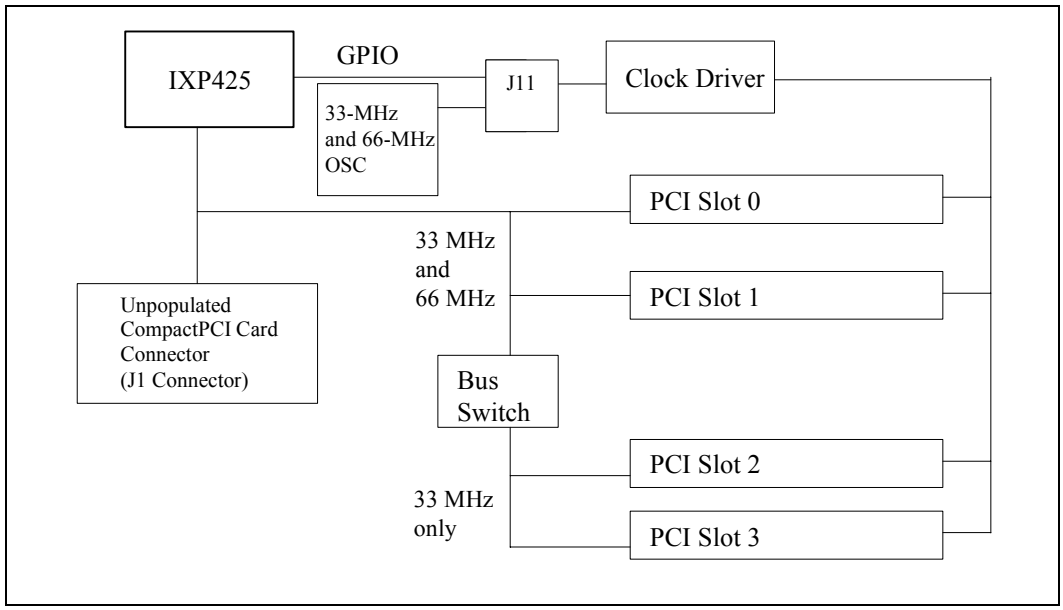
Refer to the *Intel® IXP4XX Product Line and the IXC1100 Control Plane Processor Developer's Manual* to see how to connect to SDRAM with 8-, 16-, 32-, 64-, or 128-Mbyte memory sizes.

Figure 5. 256 Mbyte – Dual Physical Bank SDRAM Interface Configuration (x16)



3.4 PCI

Figure 6. PCI Architecture



The IXP425 network processor PCI interface (Sheet 5) is a 32-bit 66 MHz/ 33 MHz PCI controller and PCI bus compatible with PCI v2.2 specification. The PCI controller is capable of operating as either a host, with internal built in PCI arbiter and PCI initiator capabilities, or an option, with target capabilities to connect to external PCI arbiter and PCI initiator. Initiator or target operations can be supported by the IXP425 Network Processor PCI controller and bus irrelevant of the configuration of the network processor.

The BIXMB425BD base card operates as a PCI Host with support for four standard +3V3 PCI connectors (Sheet 19, 20, 22, 23 - PCI slot 0,1,2,3):

- Both 33 MHz or 66 MHz PCI v2.2 bus operations are supported but not supported simultaneously. The first two slots, PCI Slot 0 and PCI Slot 1, (66 MHz and 33 MHz capable) are always seen by the IXP425 Network Processor. The other two slots, PCI Slot 2 and PCI Slot 3, (33 MHz capable) are connected through bus switches. The limitation to 2 slots at 66MHz is due to load requirements to maintain PCI signals integrity at the higher frequency. The bus switches will disable the 33 MHz PCI Slots 2 and 3 when 66 MHz PCI operation is used. Control of the bus switches is transparent to the user. The user's settings for 33 MHz/66 MHz will control whether the bus switches are on or off.
- The IXP425 network processor can drive the PCI Clock on the four PCI slots on BIXMB425BD base card through GPIO14 (PCI_CLK_FROM_CJ) and a clock driver (FS6108). The maximum clock speeds that the GPIO14 can drive is 33 MHz. Alternative PCI clocking is provided so that both 33 MHz or 66 MHz PCI interface can be driven to the PCI slots from onboard 33 MHz and 66 MHz oscillators. These oscillators, 33.0 MHz or 66.0 MHz operation is selectable through J11 jumper setting (Sheet 26 – PCI clock distribution).
- A PCI arbiter internal to the IXP425 network processor is utilized, so an external arbiter is not used for the connection to the four PCI devices.

- Reset is driven to PCI devices from reset circuitry on the BIXMB425BD base card (Sheet 27 – reset circuitry).
- All four PCI interrupts (PCI_INTA_N - PCI_INTD_N) are routed to each slot (PCI Slot 0, Slot 1, Slot 2, Slot 3). The assignment of these interrupts to each connector are rotated so that if a PCI card on a particular slot is attempting to interrupt the IXP425 network processor, there will be only one active interrupt on one of the four interrupt signals.
- A mini-PCI interface may be achieved through a mini-PCI to PCI adapter card. This adapter card can be plugged into any of the BIXMB425BD base card PCI connectors. This allows wireless LAN (IEEE 802.11x) card interface.
- The Initialization Device Select (IDSEL) signals of each of the PCI slots are mapped to the PCI address and data bus (PCI_AD) signals as shown in Table 5. The respective PCI slot is selected if the PCI address and data bus signal mapped to the particular PCI Slot IDSEL signal is asserted.

Table 5. IDSEL Mappings

Device	IDSEL Signal
Slot 0 (host mode)	PCI_AD31
Slot 1 (host mode)	PCI_AD30
Slot 2 (host mode)	PCI_AD29
Slot 3 (host mode)	PCI_AD28
IXP425 Network Processor (option mode)	CPCI_IDSEL

3.4.1 Configuring PCI Operation to 33 or 66 MHz

The platform is shipped with 33 MHz PCI Operation. The configuration settings for 33/66 MHz PCI Operation are shown in Table 6. The PCI Slots available during 33/66 MHz operation are shown in Table 7.

Table 6. Jumper Setting Descriptions for 33/66 MHz Operation

Reference	33 MHz Operation Setting	66 MHz Operation Setting
SW4 Clock Speed of the PCI Interface	SW4.5 ‘Low’	SW4.5 ‘High’
JP3 PCI Slot Configuration –	‘Shunt 2-3’	‘Shunt 1-2’
J11 PCI Clock –	‘Shunt 3-4’	‘Shunt 5-6’

Table 7. PCI Slots During 33/66 MHz Operation

PCI Slot	33 MHz Operation	66 MHz Operation
0	33 MHz capable	66 MHz capable
1	33 MHz capable	66 MHz capable
2	33 MHz capable	(Should not be populated)
3	33 MHz capable	(Should not be populated)

3.4.2 Configuring the PCI Bus for Option Mode Operation

When the IXP425 network processor is required to be a PCI option device, several changes need to take place on the BIXMB425BD base card:

- The BIXMB425BD base card should be populated with devices and compactPCI card edge connector (J20) that supports plug in to a compactPCI v2.1 interface backplane (Sheet 24 – compactPCI connector).
- The PCI slots and all associated PCI host circuitry must be depopulated on the BIXMB425BD Base card (Sheet 18, 19, 20, 21, 22, 23) except the PCI bus pull ups (Sheet 25).
- The internal PCI arbiter should be disabled. The PCI_REQN0 and PCI_GNT0 of the IXP425 network processor should be connected to external PCI arbiter through the compactPCI connector.
- Reset should be driven to the IXP425 network processor through the compactPCI connector. This reset will cause a full BIXMB425BD base card reset.
- The PCI clock should be driven externally through the compactPCI card to PCI_CLKIN. PCI_CLKIN can operate up to 66 MHz. JP8 should be set accordingly for 66 MHz/ 33 MHz mode operation.
- The PCI_IDSEL signal of the IXP425 network processor should be connected to the IDSEL signal coming in from the connector that connects to the PCI Host. Table 5 shows this IXP425 network processor as PCI option mode IDSEL mapping.

3.4.3 Design Notes

- GPIOs (GPIO[11:8]) of the Intel® IXP425 Network Processor are used by PCI devices on PCI slot 0,1,2 and 3 to interrupt the IXP425 network processor PCI controller to gain access to the PCI interface.
- PCI_INTA_N is used to request an interrupt from an external PCI host in the case if IXP425 network processor acts as a compactPCI device. PCI_INTA_N pin is tied high on BIXMB425BD design because PCI_INTA_N is an open drain pin. An interrupt to a PCI host will pull the line down. After the interrupt has happened, the line is pulled up again.
- PCI Bus Pull-ups (Sheet 25 – PCI Bus pull ups) are always required on the respective pulled up signals as required by the PCI v2.2 specification. The pull-ups are necessary because the signals are tri-stateable signals. No pull-ups are necessary on the PCI_AD lines if the PCI host interface on the IXP425 network processor is used.
- The 66 MHz-capable indication LED (DL7) will light to indicate 66 MHz PCI bus operation. The PCI Slot needs to be configured accordingly using JP3 (Sheet 25 – PCI Slot configuration) and J11 to control the PCI clock frequency. (See Table 6.)

3.5 Expansion Bus

The Intel® IXP425 Network Processor has a 16-bit data bus, and 24-bit address bus for each of its eight independent chip selects. This allows an addressing range of 512 bytes to 16 Mbyte and connection of up to eight independent external devices. Several configuration straps are implemented on the address bus of the Expansion Bus Interface.

The BIXMB425BD base card includes the following devices on the expansion bus:

- Flash boot ROM (Sheet 12)
- HSS Connectors (HSS-0, HSS-1) (Sheet 10, 11)
- ADSL Card (UTOPIA-2 connector) (Sheet 9)
- HEX Display (Sheet 13)
- Ethernet Cards via MII connectors (Ethernet-0, Ethernet-1) (Sheet 8)
- Configuration Straps (Sheet 14)

Expansion bus chip selects are used as stated below on the BIXMB425BD base card.

Table 8. Chip Select Assignments

EX_CS0_N0	Flash (FLASH_CS_N)
EX_CS0_N1	UTOPIA Card (DSL_CS_N)
EX_CS0_N2	Hexadecimal Display (HEXDISP_CS_N)
EX_CS0_N3	Test Point
EX_CS0_N4	ENET0_CS_N
EX_CS0_N5	ENET1_CS_N
EX_CS0_N6	HSS1_CS_N
EX_CS0_N7	HSS0_CS_N

The maximum address space for each chip select is 16 MBytes. The chip selects are routed through zero ohm resistors (sheet 4). If a chip select is needed for a different device, the resistor may be depopulated and the signal is routed from the resistor to the new device using a jumper wire.

A clock input (EXPB_CLK_TO_CJ) is required for the expansion bus clock interface (EX_CLK), and the maximum clock supported is 33 MHz. On the BIXMB425BD base card, GPIO15 provides a programmable CLK input (EXPB_CLK_FROM_CJ) to the expansion bus (EX_CLK) at speeds of up to 33 MHz through a clock driver (Sheet 26 – Expansion Bus Clock Distribution).

A jumper selection, JP6 is also provided on the expansion bus clock distribution circuitry to source the clock from a 33 MHz oscillator on the base card. The clock driver drives the clocks at ENET-0, ENET-1, UTOPIA-2, HSS-0, and HSS-1 connectors.

3.5.1 Configuration Straps

The expansion bus address lines (EXPB_ADDR[23:0]) are used as configuration strapping options during boot-up or whenever the reset is de-asserted. (sheet 14 – Configuration Straps) At the first cycle after the deassertion of reset, the values on these lines are read (the Expansion bus address outputs lines are switched to inputs) to determine BIXMB425BD base card and its plug-in cards configuration. These values are captured and stored in Configuration Register 0, bit [23:0].

More information about Configuration Register 0 can be found in the *Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Developer's Manual*.

SPST dip switches are placed on the BIXMB425BD base card to allow the choice of a 10-KΩ pull-down on the expansion bus address lines. The silk screens near the switches SW2, SW3, and SW4, Figure 2, are labeled 'Low' and 'High.'

Note: A 'Low' on the silkscreen indicates that the address signal is connected to the pull down register, '0.' A 'High' on the screen indicates that the address signal is connected to the pull up register, '1.' Configuration straps may be set on the base card to identify the card type on each card connector (UTOPIA, ENET-0, ENET-1, HSS-0, HSS-1).

Table 9. Configuration Strappings (Sheet 1 of 2)

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>[23:21]</td><td>Intel XScale core Clock Set[2:0]</td><td>Allow a slower Intel XScale core clock speed to override device factory settings of the on-board, 533-MHz IXP425 network processor.
<table>
<tr><th>Part in Processor socket</th><th>Desired Frequency</th><th>SW2[8: 7: 6] Setting</th></tr>
<tr><td rowspan="3">IXP420BD, IXP425BD or IXC1100BD</td><td>533 MHz</td><td>[High: High: High] (default)</td></tr>
<tr><td>400 MHz</td><td>[Low: Low: High]</td></tr>
<tr><td>266 MHz</td><td>[Low: High: High]</td></tr>
<tr><td rowspan="2">IXP420BC, IXP425BC, or IXC1100BC</td><td>400 MHz</td><td>[High: High: High]</td></tr>
<tr><td>266 MHz</td><td>[Low: High: High]</td></tr>
<tr><td>IXP420BB, IXP421BB, IXP422BB, IXP425BB, or IXC1100BB</td><td>266 MHz</td><td>[High: High: High]</td></tr>
</table>
Clock speed may not be set to a higher value than the value set by the device's factory setting.</td></tr>
<tr><td>[20:18]</td><td>AVAILABLE</td><td></td></tr>
<tr><td>[17:16]</td><td>HSS0_MODE[1:0]</td><td>Identifies the HSS-0 card type
'00' – No card or unidentified card
These bits can be used per the users desire when building own cards</td></tr>
<tr><td>[15:13]</td><td>HSS1_MODE[2:0]</td><td>Identifies the HSS-1 card type and number of cards
'000' – No card or unidentified card
These bits can be used per the users desire when building own cards.</td></tr>
</table>

Table 9. Configuration Strappings (Sheet 2 of 2)

Bit	Name	Description
[12:11]	MII1_MODE[1:0]	Identifies the MII-1 card type '00' – No card or unidentified card '01' – LXT972A These bits can be used per the users desire when building own cards.
[10:9]	MII0_MODE[1:0]	Identifies the MII-0 card type '00' – No card or unidentified card '01' – LXT972A These bits can be used per the users desire when building own cards
[8:6]	DSL_MODE[2:0]	Identifies the DSL card type '000' – No card or unidentified card '001' – Alcatel* 20150 ADSL Annex A These bits can be used per the users desire when building own cards.
[5]	RESERVED	No connection may be made – Internal only strap.
[4]	PCI_CLK	Sets the clock speed of the PCI Interface '0' – 33 MHz '1' – 66 MHz
[3]	RESERVED	No connection may be made – Internal only strap.
[2]	PCI_ARB	Enables the IXP425 network processor arbiter '0' – IXP425 network processor arbiter disabled '1' – IXP425 network processor arbiter enabled (default)
[1]	PCI_HOST	Configures the IXP425 network processor as PCI Bus Host '0' – IXP425 network processor as option '1' – IXP425 network processor as host (default)
[0]	8/16 FLASH	Specifies the data bus width of the FLASH memory device '0' – 16-bit data bus (default) '1' – 8-bit data bus 0 ohm resistor must be depopulated on EXPB_ADDR0 if 8 bit data access flash is used.

3.5.2 Hexadecimal Display

A 4-digit, 16-bit hexadecimal display is provided on the expansion bus to display the hexadecimal value that exist on the expansion bus data lines during run time (Sheet 13 – HEX Display). This display is very useful for software debugging purposes.

EX_DATA[15:0] are used to drive the hex displays. An expansion bus chip select, EXPB_CS_N2 is allocated as the latch enable signal HEXDISP_CS_N. The hexadecimal display is used by writing out data on the expansion bus and asserting the chip select EXPB_CS_N2 (see Table 8). The display writes out the hexadecimal value received on its input signals.

3.5.3 Design Notes

- EX_RDY_N[3:0] are HPI interface ready signals. If a voice card that requires HPI interface is used with the BIXMB425BD base card, the chip selects for the card must be assigned by EX_CS_N[7:4] because these chip selects are designated for HPI use. EX_RDY_N[3:0] are only affected by EX_CS_N[7:4].
- EX_IOWAIT_N signals coming out of each card (DSL_IOWAIT_N, HSS1_IOWAIT_N, HSS0_IOWAIT_N, ENET0_IOWAIT_N, ENET1_IOWAIT_N) must be open drain outputs to EX_IOWAIT_N of the IXP425 network processor (Sheet 4). EX_IOWAIT_N are affected by all expansion bus chip selects (EX_CS_N[7:0]).
- A large number of loads are present on the expansion bus. The IXP425 network processor has been tuned to drive up to eight loads, but the devices on the expansion bus may not be able to quickly drive the large load. In order to account for this, timings on the expansion bus may be adjusted using registers internal to the IXP425 network processor. If an edge rises slowly due to a low drive strength, The IXP425 network processor should wait an extra cycle before the value is read. No buffers are used to increase drive strength on the expansion bus on the BIXMB425BD base card.

3.6 Boot ROM

The Boot ROM of the IXDP425 / IXCDP1100 platform is the flash memory. Flash memory is connected through the expansion bus. The flash used is the Intel StrataFlash E28F128J3A-150 16MB, 16 bit flash in the 56-TSOP package. Intel E28F128J3A is part of the 0.25µ 3.3V Intel StrataFlash memory. The Flash is organized as 16 MBytes or 8 Mwords (128Mbit) or one-hundred-twenty-eight 128-KByte (131, 072 Bytes) erase blocks. The E28F128J3A supports the common flash interface (CFI).

More information about the E28F128J3A Intel StrataFlash Memory can be found in the *3-Volt Intel StrataFlash® Memory 28F128J3A (x8/x16) Datasheet*.

Flash is socketed on the BIXMB425BD base card, and therefore may be removed to be externally programmed with a flash programmer. The chip select of the IXP425 Network Processor expansion bus assigned to this Boot ROM is EX_CS_N0 (see Table 8).

Up to two separate images may be written into the flash, one at address 0000_0000h and one at address 0080_0000h (8-MB increment). The boot image is chosen by changing the location of the boot address. The IXP425 Network Processor will always request a starting boot address of 0000_0000h on EXPB_ADDR[23:0] as the default address. A jumper, JP11 on BIXMB425BD controls whether the exact address sent by the IXP425 Network Processor is used by the flash or if that address is hex inverted to access an increment of 8MB on the flash boot start address. (Sheet 12 – Boot ROM).

The jumper setting configurations are shown in Table 10.

Table 10. Flash Boot Address Jumper Settings (JP11)

Shunt	FLASH_ADDR23	Flash boot start address	Increment
2-3	High	0080 0000h	8 MByte
1-2	EXPB_ADDR23 (low)	0000 0000h	0 MByte

Connections to the flash chip should be as follows:

Table 11. Flash Connections (Sheet 1 of 2)

StrataFlash Pin Number	Strataflash Pin Name	Connect to	BIXMB425BD Signal Name
1	A22	IXP425 Network Processor	EXPB_ADDR22
2	CE1	GND	GND
3	A21	IXP425 Network Processor	EXPB_ADDR21
4	A20	IXP425 Network Processor	EXPB_ADDR20
5	A19	IXP425 Network Processor	EXPB_ADDR19
6	A18	IXP425 Network Processor	EXPB_ADDR18
7	A17	IXP425 Network Processor	EXPB_ADDR17
8	A16	IXP425 Network Processor	EXPB_ADDR16
9	VCC	+3V3	+3V3
10	A15	IXP425 Network Processor	EXPB_ADDR15
11	A14	IXP425 Network Processor	EXPB_ADDR14
12	A13	IXP425 Network Processor	EXPB_ADDR13
13	A12	IXP425 Network Processor	EXPB_ADDR12
14	CE0	IXP425 Network Processor	FLASH_CS_N
15	VPEN	+3V3	+3V3
16	RP#	Reset logic	RST_N
17	A11	IXP425 Network Processor	EXPB_ADDR11
18	A10	IXP425 Network Processor	EXPB_ADDR10
19	A9	IXP425 Network Processor	EXPB_ADDR9
20	A8	IXP425 Network Processor	EXPB_ADDR8
21	GND	GND	GND
22	A7	IXP425 Network Processor	EXPB_ADDR7
23	A6	IXP425 Network Processor	EXPB_ADDR6
24	A5	IXP425 Network Processor	EXPB_ADDR5
25	A4	IXP425 Network Processor	EXPB_ADDR4
26	A3	IXP425 Network Processor	EXPB_ADDR3
27	A2	IXP425 Network Processor	EXPB_ADDR2
28	A1	IXP425 Network Processor	EXPB_ADDR1
29	CE2	GND	GND
30	A23	JP11	FLASH_ADDR23
31	BYTE#	+3V3 through 10Kohm res	
32	A0	IXP425 Network Processor	EXPB_ADDR0
33	DQ0	IXP425 Network Processor	EXPB_D0
34	DQ8	IXP425 Network Processor	EXPB_D8
35	DQ1	IXP425 Network Processor	EXPB_D1
36	DQ9	IXP425 Network Processor	EXPB_D9

Table 11. Flash Connections (Sheet 2 of 2)

StrataFlash Pin Number	Strataflash Pin Name	Connect to	BIXMB425BD Signal Name
37	VCC	+3V3	+3V3
38	DQ2	IXP425 Network Processor	EXPB_D2
39	DQ10	IXP425 Network Processor	EXPB_D10
40	DQ3	IXP425 Network Processor	EXPB_D3
41	DQ11	IXP425 Network Processor	EXPB_D11
42	GND	GND	GND
43	VCCQ	+3V3	+3V3
44	DQ4	IXP425 Network Processor	EXPB_D4
45	DQ12	IXP425 Network Processor	EXPB_D12
46	DQ5	IXP425 Network Processor	EXPB_D5
47	DQ13	IXP425 Network Processor	EXPB_D13
48	GND	GND	GND
49	DQ6	IXP425 Network Processor	EXPB_D6
50	DQ14	IXP425 Network Processor	EXPB_D14
51	DQ7	IXP425 Network Processor	EXPB_D7
52	DQ15	IXP425 Network Processor	EXPB_D15
53	STS	+3V3 through 10Kohm res	FLASH_STS
54	OE#	IXP425 Network Processor	EXPB_RD_N
55	WE#	IXP425 Network Processor	EXPB_WR_N
56	A24	No connect	N/A

The size of the data transfer (8 bit or 16 bit) is set using the EXPB_ADDR0 configuration strapping jumper. (See Section 3.5.1). If the EXPB_ADDR0 strap is set to 0 at the de-assertion of RST_N, then the IXP425 Network Processor will assume an 16-bit data bus on the expansion bus. This setting is the implementation of BIXMB425BD base card. A 16-bit flash boot ROM load is required. If EXPB_ADDR0 is set to 1 at the de-assertion of reset, then the IXP425 Network Processor will use a 8-bit data bus.

Table 12. Flash Data Mode Operation

EXPB_ADDR0	Flash Data Mode Operation	FLASH_BYTE_N
0	16 bit (x16)	High
1	8 bit (x8)	Low

Flash requires a constant input on its BYTE# pin to set the data transfer size. A value of ‘0’ specifies 8-bit operation and ‘1’ specifies 16-bit operation. This pin is tied to high on the BIXMB425BD.

The FLASH_STS pin on the flash is unused on the IXP425 Network Processor. It is pulled high through a 10-KΩ resistor since it is an open drain output of the boot ROM.

A LED, DL24, will light when flash is being written. A N-channel Field Effect Transistor (FET) will perform a logic "NOR" operation of FLASH_CS_N (EXPB_CS_N0) and EXPB_WR_N and the LED will light when both FLASH_CS_N and EXPB_WR_N are low (sheet 13 – Board Status Indicator).

3.7 Card Connectors

3.7.1 UTOPIA-2 Connector

The Intel® IXP425 Network Processor has an integrated UTOPIA-2 interface that is compliant with revision 1.0 of the ATM Forum, UTOPIA Level 2 specification. The UTOPIA-2 interface can be configured to operate in a single PHY or a multi PHY selection.

More information on the IXP425 Network Processor UTOPIA-2 interface is available in the *Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Developer's Manual*.

UTOPIA-2 and Expansion Bus signals from the IXP425 Network Processor are routed to a 2x60-pin daughter card connector (J15) on the BIXMB425BD base card to allow a variety of UTOPIA PHY compliant cards to be configured and interfaced (Sheet 9 – UTOPIA-2 connector). The Expansion bus chip select use for this connector (and card) is EXPB_CS_N1 (See Table 8).

+12 V, +5 V, +3V3 and +2V5 voltages are available on the connector. A gasp circuit is implemented to give early warning of a power failure. The GASP_INT_N of the gasp circuit is asserted when +12 V or +5 V falls below acceptable value. This circuit is implemented on the BIXMB425BD base card. (sheet 28 – Power Regulation)

UTP_GPIO[5:0] are provided so that general purpose I/O connections between the IXP425 Network Processor and the UTOPIA PHY devices are provisioned, if they are required. Interrupts from UTOPIA-2 devices can also be sent to the IXP425 Network Processor to process through these GPIOs.

The UTOPIA output clock (UTP_OP_CLK) and input clock of the IXP425 Network Processor (UTP_IP_CLK) on the UTOPIA-2 connector are driven by a 33 MHz oscillator on the BIXMB425BD base card. (Sheet 9 – UTOPIA-2 connector). The UTOPIA transmit clock input (UTP_OP_CLK) and UTOPIA Receive clock input (UTP_IP_CLK) of IXP425 Network Processor is driven by the same 33 MHz oscillator. The 33 MHz oscillator can be disabled by setting appropriate JP12 setting, in case if an oscillator already exist on the card itself.

Table 13. UTOPIA-2 (J15) Connector (Sheet 1 of 3)

Pin	Signal Names on BIXMB425BD	Signal type	Pin	Signal Names on BIXMB425BD	Signal type
1	+12VD	Power	2	+12VD	Power
3	DGND	Ground	4	DGND	Ground
5	DSL_INT_N	O	6	EXPB_ADDR0	I
7	DGND	Ground	8	EXPB_ADDR2	I
9	EXPB_ADDR1	I	10	DGND	Ground
11	EXPB_ADDR3	I	12	EXPB_ADDR4	I
13	DGND	Ground	14	EXPB_ADDR6	I

Table 13. UTOPIA-2 (J15) Connector (Sheet 2 of 3)

Pin	Signal Names on BIXMB425BD	Signal type	Pin	Signal Names on BIXMB425BD	Signal type
15	EXPB_ADDR5	I	16	EXPB_ADDR8	I
17	EXPB_ADDR7	I	18	DGND	Ground
19	EXPB_ADDR9	I	20	EXPB_CLK_UTP	I
21	DGND	Ground	22	DGND	Ground
23	EXPB_D0	I/O	24	EXPB_D2	I/O
25	EXPB_D1	I/O	26	EXPB_D4	I/O
27	UTP_GPIO0	I/O	28	UTP_GPIO1	I/O
29	EXPB_D3	I/O	30	EXPB_D6	I/O
31	EXPB_D5	I/O	32	EXPB_D7	I/O
33	DGND	Ground	34	DGND	Ground
35	EXPB_WR_N	I	36	EXPB_RD_N	I
37	UTP_GPIO2	I/O	38	GASP_INT_N	I
39	RST_N	I	40	DSL_CS_N	I
41	DGND	Ground	42	DGND	Ground
43	EXPB_ALE	I	44	+3.3 VD	Power
45	DSL_TDI	I	46	+3.3 VD	Power
47	DSL_TDO	O	48	+3.3 VD	Power
49	DGND	Ground	50	DGND	Ground
51	+3.3 VD	Power	52	+3.3 VD	Power
53	DSL_TCK	I	54	DSL_TMS	I
55	+2.5 VD	Power	56	+2.5 VD	Power
57	DGND	Ground	58	DGND	Ground
59	EXPB_ADDR21	I	60	EXPB_ADDR22	I
61	DGND	Ground	62	DGND	Ground
63	+3.3 VD	Power	64	DSL_IOWAIT_N	O
65	+3.3 VD	Power	66	DGND	Ground
67	DGND	Ground	68	EXPB_ADDR23	I
69	UTP_IP_CLK	I	70	DGND	Ground
71	DGND	Ground	72	UTP_OP_CLK	I
73	UTP_IP_DATA1	O	74	DGND	Ground
75	Test Point		76	UTP_OP_DATA2	I
77	UTP_IP_DATA0	O	78	UTP_OP_FCO	I
79	UTP_IP_DATA2	O	80	DGND	Ground
81	UTP_IP_FCI	O	82	UTP_OP_DATA0	I
83	DGND	Ground	84	UTP_OP_DATA1	I
85	UTP_OP_DATA7	I	86	UTP_OP_DATA3	I
87	UTP_OP_DATA4	I	88	UTP_OP_DATA5	I

Table 13. UTOPIA-2 (J15) Connector (Sheet 3 of 3)

Pin	Signal Names on BIXMB425BD	Signal type	Pin	Signal Names on BIXMB425BD	Signal type
89	UTP_OP_DATA6	I	90	DGND	Ground
91	DGND	Ground	92	UTP_OP_FCI	O
93	UTP_IP_DATA7	O	94	UTP_OP_SOC	I
95	UTP_IP_DATA3	O	96	DGND	Ground
97	UTP_IP_DATA5	O	98	UTP_IP_DATA4	O
99	UTP_IP_SOC	O	100	UTP_IP_DATA6	O
101	UTP_IP_FCO	I	102	UTP_GPIO3	I/O
103	DGND	Ground	104	DGND	Ground
105	UTP_IP_ADDR4	I/O	106	UTP_OP_ADDR4	I/O
107	UTP_IP_ADDR3	I/O	108	UTP_OP_ADDR3	I/O
109	DGND	Ground	110	UTP_OP_ADDR2	I/O
111	UTP_IP_ADDR2	I/O	112	DGND	Ground
113	UTP_IP_ADDR1	I/O	114	UTP_OP_ADDR1	I/O
115	UTP_IP_ADDR0	I/O	116	UTP_OP_ADDR0	I/O
117	UTP_GPIO4	I/O	118	UTP_GPIO5	I/O
119	+5 VD	Power	120	+5 VD	Power

Another clock interface, EXPB_CLK_UTP is also available on the UTOPIA-2 connector. This clock is derived from GPIO15 or through a 33 MHz oscillator. GPIO15 can be programmed to supply the required EXPB_CLK_UTP frequency needed by the connector. The limitation to this GPIO15 clocking is that if GPIO15 has been programmed to drive a particular frequency for some expansion bus device, then the same programmed frequency will be driven by the clock driver to EXPB_CLK_UTP.

A second connector, 2x20 pin (J14) connector has been placed to allow a card to access all of the expansion bus address and data signals. Since the majority of the cards do not require the full expansion bus, the addition of this second connector is implemented.

Table 14. UTOPIA-2 (J14) Extender Connector (Sheet 1 of 2)

Pin	Name	Signal type	Pin	Name	Signal type
1	EXPB_D8	I/O	2	EXPB_D9	I/O
3	GND	Ground	4	GND	Ground
5	EXPB_D10	I/0	6	EXPB_D11	I/0
7	Test Point		8	Test Point	
9	GND	Ground	10	EXPB_D13	I
11	EXPB_D12	I/0	12	GND	Ground
13	EXPB_D14	I/0	14	EXPB_D15	I/0
15	Test Point		16	RESERVED	
17	EXPB_ADDR10	I	18	EXPB_ADDR11	I
19	GND	Ground	20	GND	Ground
21	EXPB_ADDR12	I	22	EXPB_ADDR13	I

Table 14. UTOPIA-2 (J14) Extender Connector (Sheet 2 of 2)

Pin	Name	Signal type	Pin	Name	Signal type
23	Test Point		24	Test Point	
25	EXPB_ADDR14	I	26	EXPB_ADDR15	I
27	GND	Ground	28	GND	Ground
29	EXPB_ADDR16	I	30	EXPB_ADDR17	I
31	Test Point		32	Test Point	
33	EXPB_ADDR18	I	34	GND	Ground
35	GND	Ground	36	EXPB_ADDR19	I
37	EXPB_A20	I	38	Test Point	
39	Test Point		40	Test Point	

3.7.1.1 UTOPIA-2 Connector Design Notes

Table 15 lists the pull-down resistors recommended if the ADSL card is not plugged into the UTOPIA-2 connector and the UTOPIA-2 signals are not used. (Sheet 9 – UTIOPIA-2 Connector)

Table 15. UTOPIA-2 Resistors

UTOPIA-2 Connector Signal Name	UTOPIA-2 Standard Signal Name	Pull to value	Resistor value
UTP_OP_FCI	UTP_TX_FULL/CLAV	GND	10K
UTP_IP_DATA[7:0]	UTP_RX_DATA[7:0]	GND	10K
UTP_IP_FCI	UTP_RX_CLAV	GND	10K
UTP_IP_SOC	UTP_RX_SOC	GND	10K

3.7.2 High-Speed, Serial-0 (HSS-0) and High-Speed, Serial-1 (HSS-1) Connector

The IXP425 Network Processor provides two high-speed serial interfaces (HSS-0 and HSS-1) that are each six-signal interface that supports transfer speeds from 512 KHz to 8.192 MHz. These high speed serial interfaces allow direct connection to serial framers, voice codecs or voice DSPs. They are capable of supporting various protocols based upon the implementation of the code developed for the Network processing engines.

BIXMB425BD base card implements two connectors dedicated for two high speed serial devices, HSS-0 (J18)and HSS-1 (J19) (Sheet 10, 11). These 2 connectors are located on the back side of the BIXMB425BD base card.

Each of the HSS card connector (HSS-0 or HSS-1) is a 2x60 pin connector. HSS signals (HSS-0 or HSS-1) are routed to this connector. Interrupts from HSS-0 or HSS-1 card are sent to GPIO3 or GPIO2 of the IXP425 Network Processor through HSS0_INT_N and HSS1_INT_N respectively. These interrupts should be active low, open drain coming from each HSS card. Other general purpose I/O connections from the HSS-0 or HSS-1 card can be connected to the IXP425 Network Processor using the GPIO[4:0] signals that are routed each of the connectors.

In addition, expansion bus signals are also routed to HSS-0 and HSS-1 connectors for configuration of the HSS cards purposes. These expansion bus signal pinouts are the same as on the MII connectors. This is to provide the option to design an HPI card to fit on either connectors. The chip select assigned to HSS-0 is EX_CS_N7 and to HSS-1 is EX_CS_N6. (See Table 4)

HSS-0 or HSS-1 TX and RX clocks on the connectors are supplied by the IXP425 Network Processor's High-Speed Serial Interfaces (HSS_TXCLK0, HSS_TXCLK1, HSS_RXCLK0, HSS_RXCLK1). The clocks can be configured to be supplied as input or output over these interfaces from a range of 512 KHz – 8.192 MHz.

If a separate clock interface is needed by the HSS cards, the connectors have other clock source (EXPB_CLK_HSS0, EXPB_CLK_HSS1) supplied from a clock driver driven by GPIO15. GPIO15 can be programmed accordingly to drive the clock needed by the HSS cards. The limitation to this GPIO15 clocking is that if GPIO15 has been programmed to drive a particular frequency for some expansion bus device, then the same programmed frequency will be driven by the clock driver to EXPB_CLK_HSS0, EXPB_CLK_HSS1. If specifically 33 MHz is needed for the HSS card and GPIO15 is not required to drive the 33 MHz, then the 33 MHz oscillator can be used by setting the right jumpers on JP6

Table 16. HSS-0 (J18) Connector (Sheet 1 of 2)

Pin	Name	Signal Type	Pin	Name	Signal Type
1	-64V	Power	2	-32V	Power
3	-64V	Power	4	-32V	Power
5	EXPB_D1	I/O	6	EXPB_D0	I/O
7	EXPB_D3	I/O	8	EXPB_D2	I/O
9	HSS0_GPIO0	I/O	10	HSS0_GPIO1	I/O
11	EXPB_D5	I/O	12	EXPB_D4	I/O
13	EXPB_D7	I/O	14	EXPB_D6	I/O
15	GND	Ground	16	GND	Ground
17	EXPB_D9	I/O	18	EXPB_D8	I/O
19	EXPB_D11	I/O	20	EXPB_D10	I/O
21	Test Point		22	Test Point	
23	EXPB_D13	I/O	24	EXPB_D12	I/O
25	EXPB_D15	I/O	26	EXPB_D14	I/O
27	GND	Ground	28	GND	Ground
29	EXPB_ADDR1	I	30	EXPB_ADDR0	I
31	EXPB_ADDR3	I	32	EXPB_ADDR2	I
33	EXPB_ADDR5	I	34	EXPB_ADDR4	I
35	EXPB_ADDR7	I	36	EXPB_ADDR6	I
37	GND	Ground	38	GND	Ground
39	EXPB_ADDR9	I	40	EXPB_ADDR8	I
41	EXPB_ADDR11	I	42	EXPB_ADDR10	I
43	EXPB_ADDR13	I	44	EXPB_ADDR12	I
45	EXPB_ADDR15	I	46	EXPB_ADDR14	I
47	GND	Ground	48	GND	Ground

Table 16. HSS-0 (J18) Connector (Sheet 2 of 2)

Pin	Name	Signal Type	Pin	Name	Signal Type
49	EXPB_ADDR17	I	50	EXPB_ADDR16	I
51	EXPB_ADDR19	I	52	EXPB_ADDR18	I
53	EXPB_ADDR21	I	54	EXPB_ADDR20	I
55	EXPB_ADDR23	I	56	EXPB_ADDR22	I
57	GND	Ground	58	GND	Ground
59	EXPB_CLK_HSS0	I	60	EXPB_RD_N	I
61	GND	Ground	62	EXPB_WR_N	I
63	EXPB_ALE	I	64	EXPB_HRDY_N3	O
65	HSS0_IOWAIT_N	O	66	HSS0_INT_N/ +3V3 through 10K resistor	OD
67	HSS0_CS_N	I	68	+3V3	Power
69	Test Point		70	+3V3	Power
71	+5V	Power	72	+3V3	Power
73	+5V	Power	74	+3V3	Power
75	+5V	Power	76	+3V3	Power
77	+5V	Power	78	+3V3	Power
79	+5V	Power	80	+3V3	Power
81	+5V	Power	82	+3V3	Power
83	HSS0_GPIO2	I/O	84	HSS0_GPIO3	I/O
85	GND	Ground	86	GND	Ground
87	HSS0_TCK	I	88	HSS0_GPIO4	I/O
89	HSS0_TDI	I	90	RST_N	I
91	HSS0_TDO	O	92	Test Point	
93	HSS0_TMS	I	94	Test Point	
95	GND	Ground	96	Test Point	
97	HSS0_TX_DATA	I	98	GND	Ground
99	HSS0_TX_FRAME	I	100	HSS0_RX_DATA	O
101	Test Point		102	HSS0_RX_FRAME	I
103	HSS0_TX_CLK	I	104	Test Point	
105	GND	Ground	106	HSS0_RX_DATA	I
107	Test Point		108	GND	Ground
109	Test Point		110	Test Point	
111	Test Point		112	Test Point	
113	+12V	Power	114	+2V5	Power
115	+12V	Power	116	+2V5	Power
117	+12V	Power	118	+2V5	Power
119	+12V	Power	120	+2V5	Power

Table 17. HSS-1 (J19) Connector Table (Sheet 1 of 2)

Pin	Name	Signal type	Pin	Name	Signal Type
1	-64V	Power	2	-32V	Power
3	-64V	Power	4	-32V	Power
5	EXPB_D1	I/O	6	EXPB_D0	I/O
7	EXPB_D3	I/O	8	EXPB_D2	I/O
9	HSS1_GPIO0	I/O	10	HSS1_GPIO1	I/O
11	EXPB_D5	I/O	12	EXPB_D4	I/O
13	EXPB_D7	I/O	14	EXPB_D6	I/O
15	GND	Ground	16	GND	Ground
17	EXPB_D9	I/O	18	EXPB_D8	I/O
19	EXPB_D11	I/O	20	EXPB_D10	I/O
21	Test Point		22	Test Point	
23	EXPB_D13	I/O	24	EXPB_D12	I/O
25	EXPB_D15	I/O	26	EXPB_D14	I/O
27	GND	Ground	28	GND	Ground
29	EXPB_ADDR1	I	30	EXPB_ADDR0	I
31	EXPB_ADDR3	I	32	EXPB_ADDR2	I
33	EXPB_ADDR5	I	34	EXPB_ADDR4	I
35	EXPB_ADDR7	I	36	EXPB_ADDR6	I
37	GND	Ground	38	GND	Ground
39	EXPB_ADDR9	I	40	EXPB_ADDR8	I
41	EXPB_ADDR11	I	42	EXPB_ADDR10	I
43	EXPB_ADDR13	I	44	EXPB_ADDR12	I
45	EXPB_ADDR15	I	46	EXPB_ADDR14	I
47	GND	Ground	48	GND	Ground
49	EXPB_ADDR17	I	50	EXPB_ADDR16	I
51	EXPB_ADDR19	I	52	EXPB_ADDR18	I
53	EXPB_ADDR21	I	54	EXPB_ADDR20	I
55	EXPB_ADDR23	I	56	EXPB_ADDR22	I
57	GND	Ground	58	GND	Ground
59	EXPB_CLK_HSS1	I	60	EXPB_RD_N	I
61	GND	Ground	62	EXPB_WR_N	I
63	EXPB_ALE	I	64	EXPB_HRDY_N3	O
65	HSS0_IOWAIT_N	O	66	HSS1_INT_N/ +3V3 through 10K resistor	OD
67	HSS0_CS_N	I	68	+3V3	Power
69	Test Point		70	+3V3	Power
71	+5V	Power	72	+3V3	Power

Table 17. HSS-1 (J19) Connector Table (Sheet 2 of 2)

Pin	Name	Signal type	Pin	Name	Signal Type
73	+5V	Power	74	+3V3	Power
75	+5V	Power	76	+3V3	Power
77	+5V	Power	78	+3V3	Power
79	+5V	Power	80	+3V3	Power
81	+5V	Power	82	+3V3	Power
83	HSS1_GPIO2	I/O	84	HSS1_GPIO3	I/O
85	GND	Ground	86	GND	Ground
87	HSS1_TCK	I	88	HSS1_GPIO4	I/O
89	HSS1_TDI	I	90	RST_N	I
91	HSS1_TDO	O	92	Test Point	
93	HSS1_TMS	I	94	Test Point	
95	GND	Ground	96	Test Point	
97	HSS1_TX_DATA	I	98	GND	Ground
99	HSS1_TX_FRAME	I	100	HSS1_RX_DATA	O
101	Test Point		102	HSS1_RX_FRAME	I
103	HSS1_TX_CLK	I	104	Test Point	
105	GND	Ground	106	HSS1_RX_DATA	I
107	Test Point		108	GND	Ground
109	Test Point		110	Test Point	
111	Test Point		112	Test Point	
113	+12V	Power	114	+2V5	Power
115	+12V	Power	116	+2V5	Power
117	+12V	Power	118	+2V5	Power
119	+12V	Power	120	+2V5	Power

3.7.2.1 High-Speed, Serial Connector Design Notes

HSS0_INT_N0 and HSS_INT_N1 are interrupts coming in from the HSS-0 and the HSS-1 card that should be active low and open drain. So, a pull-up is required on the lines for each of the interrupts to be asserted.

The following table lists the pull-up and pull-down resistors placed on the BIXMB425BD base card just for the case that the HSS-0 / HSS-1 interface is not used and there is no card plugged into the HSS-0 / HSS-1 connectors. The 10-KΩ resistors were chosen so that the HSS cards can easily drive over the pull- downs when the cards are used.

Table 18. HSS-0 Resistors

Signal	Pull to value	Resistor value
HSS0_TXDATA	+3 V3	10 KΩ
HSS0_TXFRAME	GND	10 KΩ
HSS0_TXCLK	GND	10 KΩ
HSS0_RXDATA	GND	10 KΩ
HSS0_RXFRAME	GND	10 KΩ
HSS0_RXCLK	GND	10 KΩ

Table 19. HSS-1 Resistors

Signal	Pull to value	Resistor value
HSSV_TXDATA1	+3 V3	10 KΩ
HSSV_TXFRAME1	GND	10 KΩ
HSSV_TXCLK1	GND	10 KΩ
HSSV_RXDATA1	GND	10 KΩ
HSSV_RXFRAME1	GND	10 KΩ
HSSV_RXCLK1	GND	10 KΩ

HSS0_TX_DATA and HSS1_TX_DATA are open drain outputs from the IXP425 Network Processor. So, pull ups are required if the HSS0 or HSS1 cards are not plugged into the connectors.

3.7.3 ENET-0 / ENET-1 Connectors

The IXP425 Network Processor has two integrated 10/100 MAC with two industry standard Media Independent Interfaces (MII). The IXP425 Network Processor includes a single Management Data Interface – Management Data Input Output (MDIO) and Management Data Clock (MDC). The MII interfaces and the single management data interface are used to communicate, control and configure PHY devices.

BIXMB425BD base card integrates support for the IXP425 Network Processor's two MIIs through two MII connectors, ENET-0 (J13) and ENET-1 (J6) (sheet 8). The connector used on the base card for each MII is 2x60 pin. Both connectors are identical in signal types routed to them. Because of this, similar cards may be used on both MII connectors. ENET_MDC and ENET_MDIO from the IXP425 Network Processor are routed to both MII connectors. It is the responsibility of the card to guarantee a different address on each connector. The chip selects (ENET0_CS_N, ENET1_CS_N) on the IXP425 Network Processor expansion bus assigned to ENET-0 is EX_CS_N4 and ENET-1 is EX_CS_N5 (See Table 8). Because the IXP425 Network Processor ENET-1 MAC/Network Processing Engine B supports ethernet MAC hashing, ENET-1 connector supports this hashing capability. ENET-0 does not have this capability.

A card containing a single IEEE 802.3 standard Ethernet PHY with MII interface (for single ethernet or multi ethernet port), wireless LAN, Home PNA, switch, or repeater may be supported on each connector.

The 25-MHz (for 100-Mbps operation) / 2.5-MHz (for 10-Mbps operation) clocks for TX and RX MII interface (ENET_TX_CLK, ENET_RX_CLK) for each ENET card are expected to be supplied from oscillators on the cards themselves. Each of the TX and RX clock are then supplied to the IXP425 Network Processor's respective MII / RMII (ETH_TXCLK0, ETH_RXCLK0, ETH_TXCLK1, ETH_RXCLK1) interface through the connectors. (Sheet 8 – Ethernet Connectors)

Each connector also has alternative clock interface. (EXPB_CLK_ENET0, EXPB_CLK_ENET1). These clocks are derived from a clock driver through a programmable GPIO15 clock supply. The limitation to this GPIO15 clocking is that if GPIO15 has been programmed to drive a particular frequency for some expansion bus device, then the same frequency will be driven by the clock driver to EXPB_CLK_ENET0, EXPB_CLK_ENET1. An option for clock to be driven from an external 33MHz oscillator is also provided.through the same clock driver. (Sheet 26 – Expansion Bus Clock Distribution).

Active low, open drain interrupts from the ENET-0 and ENET-1 cards (ENET0_INT_N, ENET1_INT_N) are supported by GPIO4 and GPIO5. (Sheet 15 – GPIO Routing, GPIO Header A). Each of these signals is pulled high on each connector, so that if an interrupt has been asserted when an ENET device (on either ENET-0 or ENET-1 card) wants to interrupt the IXP425 Network Processor, the signal can return to its high position for another active low interrupt to happen.

Expansion bus signals are routed to the connectors for configuration and interface of the ENET-0 and ENET-1 card purposes. Additional GPIO pins are also provided to the connectors for generic I/O of the Ethernet devices on ENET-0 or ENET-1 to the IXP425 Network Processor.

Table 20. ENET-0 (J13) Connector (Sheet 1 of 3)

Pin	Name	Signal type	Pin	Name	Signal type
1	-64V	Power	2	-32V	Power
3	-64V	Power	4	-32V	Power
5	EXPB_D1	I/O	6	EXPB_D0	I/O
7	EXPB_D3	I/O	8	EXPB_D2	I/O
9	ENET0_GPIO0	I/O	10	ENET0_GPIO1	I/O
11	EXPB_D5	I/O	12	EXPB_D4	I/O
13	EXPB_D7	I/O	14	EXPB_D6	I/O
15	GND	Ground	16	GND	Ground
17	EXPB_D9	I/O	18	EXPB_D8	I/O
19	EXPB_D11	I/O	20	EXPB_D10	I/O
21	Test Point		22	Test Point	
23	EXPB_D13	I/O	24	EXPB_D12	I/O
25	EXPB_D15	I/O	26	EXPB_D14	I/O
27	GND	Ground	28	GND	Ground
29	EXPB_ADDR1	I	30	EXPB_ADDR0	I
31	EXPB_ADDR3	I	32	EXPB_ADDR2	I
33	EXPB_ADDR5	I	34	EXPB_ADDR4	I

Table 20. ENET-0 (J13) Connector (Sheet 2 of 3)

Pin	Name	Signal type	Pin	Name	Signal type
35	EXPB_ADDR7	I	36	EXPB_ADDR6	I
37	GND	Ground	38	GND	Ground
39	EXPB_ADDR9	I	40	EXPB_ADDR8	I
41	EXPB_ADDR11	I	42	EXPB_ADDR10	I
43	EXPB_ADDR13	I	44	EXPB_ADDR12	I
45	EXPB_ADDR15	I	46	EXPB_ADDR14	I
47	GND	Ground	48	GND	Ground
49	EXPB_ADDR17	I	50	EXPB_ADDR16	I
51	EXPB_ADDR19	I	52	EXPB_ADDR18	I
53	EXPB_ADDR21	I	54	EXPB_ADDR20	I
55	EXPB_ADDR23	I	56	EXPB_ADDR22	I
57	GND	Ground	58	GND	Ground
59	EXPB_CLK_ENET0		60	EXPB_RD_N	I
61	GND	Ground	62	EXPB_WR_N	I
63	EXPB_ALE	I	64	EXPB_HRDY_N0	O
65	ENET0_IOWAIT_N	O	66	ENET0_INT_N/ 10K res to high	OD
67	ENET0_CS_N	I	68	+3V3	Power
69	Test Point		70	+3V3	Power
71	+5V	Power	72	+3V3	Power
73	+5V	Power	74	+3V3	Power
75	+5V	Power	76	+3V3	Power
77	+5V	Power	78	+3V3	Power
79	+5V	Power	80	+3V3	Power
81	+5V	Power	82	+3V3	Power
83	ENET0_GPIO2	I/O	84	ENET0_GPIO3	I/O
85	GND	Ground	86	GND	Ground
87	ENET0_TCK	I	88	ENET0_GPIO4	I/O
89	ENET0_TDI	I	90	RST_N	I
91	ENET0_TDO	O	92	ENET0_TX_EN	O
93	ENET0_TMS	I	94	ENET0_RX_DV	I
95	GND	Ground	96	ENET0_RX_CLK	I
97	ENET0_RXD3	I	98	GND	Ground
99	ENET0_RXD2	I	100	ENET0_TX_CLK	I
101	ENET0_RXD1	I	102	ENET0_COL	O
103	ENET0_RXD0	I	104	ENET0_TXD3	O
105	GND	Ground	106	ENET0_TXD2	O
107	ENET_MDC	I	108	GND	Ground

Table 20. ENET-0 (J13) Connector (Sheet 3 of 3)

Pin	Name	Signal type	Pin	Name	Signal type
109	ENET_MDIO	I/O	110	ENET0_TXD1	O
111	ENET0_CRS	O	112	ENET0_TXD0	I/O
113	+12V	Power	114	+2V5	Power
115	+12V	Power	116	+2V5	Power
117	+12V	Power	118	+2V5	Power
119	+12V	Power	120	+2V5	Power

Table 21. ENET-1 (J6) Connector (Sheet 1 of 2)

Pin	Name	Signal type	Pin	Name	Signal type
1	-64V	Power	2	-32V	Power
3	-64V	Power	4	-32V	Power
5	EXPB_D1	I/O	6	EXPB_D0	I/O
7	EXPB_D3	I/O	8	EXPB_D2	I/O
9	ENET1_GPIO0	I/O	10	ENET1_GPIO1	I/O
11	EXPB_D5	I/O	12	EXPB_D4	I/O
13	EXPB_D7	I/O	14	EXPB_D6	I/O
15	GND	Ground	16	GND	Ground
17	EXPB_D9	I/O	18	EXPB_D8	I/O
19	EXPB_D11	I/O	20	EXPB_D10	I/O
21	Test Point		22	Test Point	
23	EXPB_D13	I/O	24	EXPB_D12	I/O
25	EXPB_D15	I/O	26	EXPB_D14	I/O
27	GND	Ground	28	GND	Ground
29	EXPB_ADDR1	I	30	EXPB_ADDR0	I
31	EXPB_ADDR3	I	32	EXPB_ADDR2	I
33	EXPB_ADDR5	I	34	EXPB_ADDR4	I
35	EXPB_ADDR7	I	36	EXPB_ADDR6	I
37	GND	Ground	38	GND	Ground
39	EXPB_ADDR9	I	40	EXPB_ADDR8	I
41	EXPB_ADDR11	I	42	EXPB_ADDR10	I
43	EXPB_ADDR13	I	44	EXPB_ADDR12	I
45	EXPB_ADDR15	I	46	EXPB_ADDR14	I
47	GND	Ground	48	GND	Ground
49	EXPB_ADDR17	I	50	EXPB_ADDR16	I
51	EXPB_ADDR19	I	52	EXPB_ADDR18	I
53	EXPB_ADDR21	I	54	EXPB_ADDR20	I
55	EXPB_ADDR23	I	56	EXPB_ADDR22	I
57	GND	Ground	58	GND	Ground

Table 21. ENET-1 (J6) Connector (Sheet 2 of 2)

Pin	Name	Signal type	Pin	Name	Signal type
59	EXPB_CLK_ENET1		60	EXPB_RD_N	I
61	GND	Ground	62	EXPB_WR_N	I
63	EXPB_ALE	I	64	EXPB_HRDY_N0	O
65	ENET1_IOWAIT_N	O	66	ENET1_INT_N / 10K res to high	OD
67	ENET1_CS_N	I	68	+3V3	Power
69	Test Point		70	+3V3	Power
71	+5V	Power	72	+3V3	Power
73	+5V	Power	74	+3V3	Power
75	+5V	Power	76	+3V3	Power
77	+5V	Power	78	+3V3	Power
79	+5V	Power	80	+3V3	Power
81	+5V	Power	82	+3V3	Power
83	ENET1_GPIO2	I/O	84	ENET1_GPIO3	I/O
85	GND	Ground	86	GND	Ground
87	ENET1_TCK	I	88	ENET1_GPIO4	I/O
89	ENET1_TDI	I	90	RST_N	I
91	ENET1_TDO	O	92	ENET1_TX_EN	O
93	ENET1_TMS	I	94	ENET1_RX_DV	I
95	GND	Ground	96	ENET1_RX_CLK	I
97	ENET1_RXD3	I	98	GND	Ground
99	ENET1_RXD2	I	100	ENET1_TX_CLK	I
101	ENET1_RXD1	I	102	ENET1_COL	O
103	ENET1_RXD0	I	104	ENET1_TXD3	O
105	GND	Ground	106	ENET1_TXD2	O
107	ENET_MDC	I	108	GND	Ground
109	ENET_MDIO	I/O	110	ENET1_TXD1	O
111	ENET1_CRS	O	112	ENET1_TXD0	I/O
113	+12V	Power	114	+2V5	Power
115	+12V	Power	116	+2V5	Power
117	+12V	Power	118	+2V5	Power
119	+12V	Power	120	+2V5	Power

3.7.3.1 ENET Connector Design Notes

The table below describes the pull-downs required on the ENET connectors if the following (input signals to the IXP425 Network Processor) are not used and MII card not plugged in. The 10k resistor value was chosen so that the signals on the either card can easily drive over the pull down if they were used.

Table 22. ENET-0 / ENET-1 Resistors

Signal	Pull to value	Resistor value
ENET0_TXCLK	GND	10 KΩ
ENET0_RXCLK	GND	10 KΩ
ENET0_RXDATA[3:0]	GND	10 KΩ
ENET0_RXDV	GND	10 KΩ
ENET0_COL	GND	10 KΩ
ENET0_CRS	GND	10 KΩ
ENET_MDIO	GND	10 KΩ
ENET1_TXCLK	GND	10 KΩ
ENET1_RXCLK	GND	10 KΩ
ENET1_RXDATA[3:0]	GND	10 KΩ
ENET1_RXDV	GND	10 KΩ
ENET1_COL	GND	10 KΩ
ENET1_CRS	GND	10 KΩ

3.8 USB

The IXP425 Network Processor has integrated USBv1.1 Device Controller (UDC) interface. This UDC interface can operate as a half-duplex, slave-only device at a baud rate of 12 Mbps. This UDC interface is not a USB host, or a USB hub controller. The UDC supports full speed USB v1.1, has 16 Endpoints and has integrated transceiver.

A Type-B USB “device” receptacle (P3) is provided at the board edge. (Sheet 17 – USB Connector) A 1.5-KΩ pull-up resistor is applied on USB_D+ USB pin to indicate the IXP425 Network Processor is a full-speed USBv1.1 device and USB_D+ is correct polarity for data transmission. The USB protocol uses differential signalling between the two pins USB_D+ and USB_D- for half-duplex data transmission.

The IXP425 Network Processor cannot be powered as a downstream USB device through the USB interface. This is due to the high power requirements of the devices on BIXMB425BD base card that are interfacing to the IXP425 Network Processor.

3.9 UART Ports

The IXP425 Network Processor provides two dedicated asynchronous serial I/O ports (UARTs). There are the high speed UART and the console UART. These UARTs are 16550 compliant with the enhancement of larger 64Byte transmit and receive buffers. The Request to Send (RTS_N) and Clear to Send (CTS_N) modem control signals are provided by the IXP425 Network Processor on both UART ports.

Both ports are routed to 9-pin DB connectors with RTS and CTS flow control on the BIXMB425BD base card (Sheet 16- Serial Ports). The High-Speed UART port will include support for full modem control through 4 GPIOs if desired. The ports are wired according to the RS-232 specification for data communication equipment. Straight serial cables can be used to connect to the host PC.

A breakout of the IXP425 Network Processor's UART pins for raw access is provided through an unpopulated 2x6 header, J1. The header will have the following connections.

Table 23. Serial Port Header

Pin Number	Signal Name	Pin Number	Signal Name
1	URT0_TXD	2	+3V3
3	URT0_RXD	4	+3V3
5	URT0_RTS_N	6	URT1_TXD
7	URT0_CTS_N	8	URT1_RXD
9	GND	10	URT1_RTS_N
11	GND	12	URT1_CTS_N

3.9.1 High-Speed UART

This IXP425 Network Processor high-speed UART interface can be configured to support speeds from 1,200 Baud to 921 KBaud. This interface supports five, six, seven, or eight data-bit transfers, one or two stop bits, and even, odd or no parity configurations.

The UART signals from the IXP425 Network Processor for the fast transceiver is routed through the MAX3237 transceiver (Sheet 16 – Serial Ports) to a high-speed UART port (P2). The transceiver has five transmit and three receive signals to handle all modem control signals. For MBAUD signal, options are provided for pull up so that 1-Mbps transmission rate is achieved, or pull down so that 250 Kbps transmission rate can be set. The default setting is 1 Mbps.

To allow full modem control on the high-speed UART connection port, four GPIOs may optionally be used to generate the RS-232 signals (URT0_DTR, URT0_DSR, URT0_RI, and URT0DCD) that are not available on the IXP425 Network Processor High-Speed UART interfaces. (Sheet 15 – GPIO Header B) A jumper option implemented through GPIO Header B allows the connection of GPIOs to the UART transceiver signal lines.

Bluetooth* support may be achieved using the Bluetooth developers kit on the fast serial port. This provides a Bluetooth card that plugs into a standard nine-pin serial port.

Table 24. High-Speed UART Port Transceiver Connections

MAX3237 Pin Name	Connect to device	BIXMB425BD Base Card Signal Name for Fast UART
C2+	0.1µF cap	0.1µF cap between pin 1 and pin 3
GND		GND
C2-	0.1µF cap	0.1µF cap between pin 1 and pin 3
V-	0.1µF cap	0.1µF cap to GND
T1OUT	DB9	DCD0
T2OUT	DB9	DSR0
T3OUT	DB9	TXD0
R1IN	DB9	CTS0_N
R2IN	DB9	RXD0
T4OUT	DB9	RTS0_N
R3IN	DB9	DTR0
T5OUT	DB9	RI0
EN_N	1k res	1k pull down, with unpopulated pull-up for disable option
SHDN_N	10k res	10k pull up
MBAUD	10k pull up, with option for pull down.	Pull up for 1Mbps rate, pull down for normal operation (250kbps)
R1OUTB	N/A	Testpoint
T5IN	IXP425 Network Processor	GPIO - URT0_RI
R3OUT	IXP425 Network Processor	GPIO - URT0_DTR
T4IN	IXP425 Network Processor	URT0_RTS_N
R2OUT	IXP425 Network Processor	URT0_RXD
R1OUT	IXP425 Network Processor	URT0_CTS_N
T3IN	IXP425 Network Processor	URT0_TXD
T2IN	IXP425 Network Processor	GPIO - URT0_DSR
T1IN	IXP425 Network Processor	GPIO - URT0_DCD
C1-	0.1µF cap	0.1µF cap between pin 25 and pin 28
VCC		+3V3, 0.1µF decoupling cap to GND
V+	0.1µF cap	0.1µF cap to +3V3
C1+	0.1µF cap	0.1µF cap between pin 25 and pin 28

3.9.1.1 High-Speed UART Port Design Notes

The following configurations must be considered:

- URT0_DSR, URT0_DCD, URT0_RI are not connected to GPIOs in the default setting of BIXMB425BD base card. So, 10K resistors are placed so that inputs to transceiver will not be floating.
- When the URT0_DSR, URT0_DTR, and URT0_DCD signals are connected to the GPIOs (GPIO Header B), the 0ohm resisters between DCD0, DSR0 and DTR0 should be removed, and the 0-Ω resistors connecting DCD0, DSR0, DTR0 and RI0 to the transceiver should be populated.
- There are weak internal pull downs on receiver inputs (URT0_CTS_N, URT0_RXD, URT0_DTR). Output values are inverted from the inputs.

3.9.2 Console UART Port

The Console UART interface of the IXP425 Network Processor has the same features as the high-speed UART. The baud rate supported on the Console UART of the IXP425 Network Processor is from 1,200 Baud to 921Kbaud. The console UART port (P1) on BIXMB425BD base card will be routed to the four UART signals from the IXP425 Network Processor to the port (Sheet 16 – Serial Ports). Therefore, a smaller transceiver Maxim MAX3223 is used.

Table 25. Console UART Port Transceiver Connections (Sheet 1 of 2)

MAX3223 Pin Name	Connect to device	BIXMB425BD Base Card Signal Name for Slow UART
EN_N	10K res	10K resistor to GND, with unpopulated pull-up for disable option
C1+	0.1µF cap	0.1µF cap between pin2 and pin4
V+	0.1µF cap	0.1µF cap to GND
C1-	0.1µF cap	0.1µF cap between pin2 and pin4
C2+	0.1µF cap	0.1µF cap between pin5 and pin6
C2-	0.1µF cap	0.1µF cap between pin5 and pin6
V-	0.1µF cap	0.1µF cap to GND
T2OUT	DB9	TXD1
R2IN	DB9	RXD1
R2OUT	IXP425 Network Processor	URT1_RXD
INVALID	N/A	Testpoint
T2IN	IXP425 Network Processor	URT1_TXD
T1IN	IXP425 Network Processor	URT1_RTS_N
FORCEON	300ohm res	Pull-down through 300 ohm
R1OUT	IXP425 Network Processor	URT1_CTS_N
R1IN	DB9	CTS1_N
T1OUT	DB9	RTS1_N

Table 25. Console UART Port Transceiver Connections (Sheet 2 of 2)

MAX3223 Pin Name	Connect to device	BIXMB425BD Base Card Signal Name for Slow UART
GND	N/A	GND
VCC	N/A	+3V3
FORCEOFF_N	10K res	Pull-up through 10k

3.9.3 DB-9 Connectors

The pin-out for the DB-9 serial port UART connectors are shown in Table 26. Ferrites are used as buffers on all signals between the transceivers and the UART connectors.

Table 26. DB-9 Port Connections

UART Connector Pin Number	UART Connector Pin Name	Connect to device	BIXMB425BD Base card Signal Name for High-Speed UART	BIXMB425BD Base card Signal Name for Console UART
1	DC0	MAX3223/MAX 3237	DCD0	Connect to pins 4 and 6
2	TXD0	MAX3223/MAX 3237	TXD0	TXD1
3	RXD0	MAX3223/MAX 3237	RXD0	RXD1
4	DT0	MAX3223/MAX 3237	DTR0	Connect to pins 1 and 6
5	SG	MAX3223/MAX 3237	GND	GND
6	DS0	MAX3223/MAX 3237	DSR0	Connect to pins 4 and 1
7	CTS0_N	MAX3223/MAX 3237	CTS0_N	CTS1_N
8	RTS0_N	MAX3223/MAX 3237	RTS0_N	RTS1_N
9	RI0	MAX3223/MAX 3237	RI0	Not connected

3.10 General Purpose Input/Output (GPIO)

The IXP425 Network Processor provides 16 GPIO pins. GPIO[13:0] are general-purpose, configurable I/O pins, GPIO[12:0] can be used to capture interrupts from I/O devices connected to the GPIO interface. In addition, GPIO14 and GPIO15 can be configured as clock outputs. Clock speeds can be set at various speeds, up to 33 MHz, with various duty cycles.

The GPIOs are mapped to many purposes on BIXMB425BD base card (Sheet 15 – GPIO Routing). A 2x16-pin header (Header A, J17) is placed on BIXMB425BD base card with the below signals as shown in table 23 routed to it. A 2x14-pin header (Header B, J16) is placed to give flexibility in routing GPIOs to any board subsystem that might need them.

To connect GPIOs to the default mapping on the BIXMB425BD base card, shunts are placed on the GPIO Header A as follows: 1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, 15-16, 17-18, 19-20, 21-22, 23-24, 25-26, 27-28, 29-30, 31-32.

To map to a signal that is not in the original mapping on the BIXMB425BD base card, the shunt may be removed from Header A, and then a wire can be routed from the GPIO signal to the desired mapping on Header B.

Table 27. GPIO Header A (J17)

Pin #	Signal	Pin #	Signal
1	GPIO15	2	Expansion Bus Clock Out (to clock driver)
3	GPIO14	4	PCI Clock Out
5	GPIO13	6	PCI Reset Out
7	GPIO12	8	UTOPIA GPIO0
9	GPIO11	10	PCI_INTA (for PCI devices to IXP425 Network Processor)
11	GPIO10	12	PCI_INTB (for PCI devices to IXP425 Network Processor)
13	GPIO9	14	PCI_INTC (for PCI devices to IXP425 Network Processor)
15	GPIO8	16	PCI_INTD (for PCI devices to IXP425 Network Processor)
17	GPIO7	18	I2C SDA
19	GPIO6	20	I2C SCL
21	GPIO5	22	Ethernet-1 Interrupt
23	GPIO4	24	Ethernet-0 Interrupt
25	GPIO3	26	HSS-0 Interrupt
27	GPIO2	28	HSS-1 Interrupt
29	GPIO1	30	UTOPIA PHY interrupt
31	GPIO0	32	UTOPIA GPIO1

Table 28. GPIO Header B (J16)

Pin #	Signal	Pin #	Signal
1	UTOPIA GPIO2	2	HSS-1 GPIO0
3	UTOPIA GPIO3	4	HSS-1 GPIO1
5	UTOPIA GPIO4	6	HSS-1 GPIO2
7	UTOPIA GPIO5	8	HSS-1 GPIO3
9	Fast Serial port DTR	10	Ethernet 0 GPIO0
11	Fast Serial port DSR	12	Ethernet 0 GPIO1
13	Fast Serial port DCD	14	Ethernet 0 GPIO2
15	Fast Serial port RI	16	Ethernet 0 GPIO3
17	HSS-0 GPIO0	18	Ethernet 0 GPIO4
19	HSS-0 GPIO1	20	Ethernet 1 GPIO0

Table 28. GPIO Header B (J16)

Pin #	Signal	Pin #	Signal
21	HSS-0 GPIO2	22	Ethernet 1 GPIO1
23	HSS-0 GPIO3	24	Ethernet 1 GPIO2
25	HSS-0 GPIO4	26	Ethernet 1 GPIO3
27	HSS-0 GPIO5	28	Ethernet 1 GPIO4

3.10.1 GPIO LEDs

The option to use the GPIOs to drive LEDs is provided through two, eight-position SPST dip switches (SW6, SW5) (Sheet 15 – LEDs). Switches allow users the flexibility for users to choose whether to connect an LED to each GPIO as needed. The switch allows the user to connect the GPIOs to LEDs and resistors tied high. “ON” connects the LED to the GPIO. This is the default setting of BIXMB425BD Base card. See Table 27 for LED indicators of these GPIO LEDs. When the switch is in the other position, the GPIOs are not connected to the LEDs.

The drive strength for GPIO[15:14] is only 8 mA, so LEDs driven by these signals are not as bright. The drive strength for GPIO [13:0] is 16mA. If it is desired to remove connection to the LED, the resistor may be removed.

3.11 I2C EEPROM

A 512-byte I2C EEPROM (Sheet 12 – I2C EEPROM) is connected to the IXP425 Network Processor through two GPIO pins, GPIO6, GPIO7 on GPIO Header A (J17). There is an option to isolate the I2C device in order to allow the GPIOs to be used for other purposes. This is accomplished through the GPIO Header A to select whether they are connected to the I2C EEPROM or not.

Table 29. I2C EEPROM Connections

I2C EEPROM Pin Number	I2C EEPROM Pin Name	Connect to	Platform-level Signal Name
1	A0	GND	GND
2	A1	GND	GND
3	A2	GND	GND
4	GND	GND	GND
5	I2C_SDA	GPIO7 through 2-pin jumper – pull up to +3V3 through 10k	I2C_SDA
6	I2C_SCL	GPIO6 through 2-pin jumper – pull up to +3V3 through 10k	I2C_SCL
7	PTC	Pull up to +3V3 through 10k	I2C_PTC
8	VCC	+3V3	+3V3

3.12 LED Indicators

The following LEDs are placed on the board as indicators:

Table 30. LED Indicators

LED	LED Indication when on	Color
Power LED (DL1)	+12 V powered up	Red
Power LED (DL2)	+5 V powered up	Red
Power LED (DL3)	+3.3 V powered up	Red
Power LED (DL4)	+2.5 V powered up	Red
Power LED (DL5)	+1.3 V powered up	Red
Reset (DL6)	System is in reset	Red
PCI 66MHz Capable (DL7)	PCI 66-MHz operation	Red
GPIO[15:14] Pull Up (DL8/DL9)	GPIO[15:14] driven through pull up	
GPIO[13:0] Pull-up LED (DL10, DL23)	GPIO[13:0] driven through pull-up	Green
Flash Burn (DL24)	Flash is being burned	Red

3.13 ICE Emulator Interface

The IXP425 Network Processor is controlled during debug through a industry standard IEEE1149.1 JTAG interface to the processor. The JTAG signals is routed to both the Test Logic Unit (TLU) within the IXP425 Network Processor and the Intel XScale core JTAG functionality (TAP Controller). The Macraigor* Raven*, ARM* Multi-ICE* and Wind River Systems* visionPROBE*/visionICE* systems can plug into the JTAG interface through a 20-pin connector, defined below (J12, Sheet 30 – ICE JTAG Port). The main difference between the Raven and visionICE systems is the specific implementation of TRST_N for each debugger. The Macraigor Raven implementation actively drives TRST_N (high and low). The Wind River Systems visionPROBE / visionICE can configure TRST_N active or open collector (only drive low). Other ICE devices may be connected using adapter connectors/cables and as long as the IXP425 Network Processor is supported by the ICE tool.

Unpopulated resistor footprints are placed along the below lines so that changes to the JTAG circuitry can quickly be made.

Table 31. ICE Emulator J12 Connector (Sheet 1 of 2)

Pin #	Pin Name	Connect To	Pin #	Pin Name	Connect To
1	VTREF	+3V3	2	VSUPPLY	+3V3
3	TRST_N	JTG_TRST_N/10k Pull-up, option for 10k Pull-down (DNP) – TRST & generated from Corelis* test equipment	4	GND	GND
5	TDI	ICE_TDI/Pull-up (DNP) or Pull-down (DNP) Option	6	GND	GND
7	TMS	ICE_TMS/10K Pull-up or 10K Pull-down Option (DNP)	8	GND	GND
9	TCK	ICE_TCK/1k Pull-up, 10K Pull-down Option (DNP)	10	GND	GND
11	RTCK	GND	12	GND	GND

Table 31. ICE Emulator J12 Connector (Sheet 2 of 2)

Pin #	Pin Name	Connect To	Pin #	Pin Name	Connect To
13	TDO	ICE_TDO	14	GND	GND
15	SRST_N	Reset circuitry/10K Pull-up or 10K Pull-down Option	16	GND	GND
17	DBGRQ	Testpoint	18	GND	GND
19	DGBACK	Testpoint	20	GND	GND

3.13.1 ICE Emulator Design Notes

Pull down resistor of 10-KΩ are provided on the JTAG port on JTG_TRST_N because there is a requirement of TRST_N to be weakly pulled down at the processor.

3.14 Power

Power rails are supplied with power on BIXMB425BD base card through the Voltage Regulator card connector J7 (Sheet 28 – Power Module Connector). The following voltages are provided: +3V3V (+3.3 V), 5 V, 12 V, +2V5 (+2.5 V), -64 V, -32 V, GND. The power sequence required by the IXP425 Network Processor is from 12 V-> 5 V-> 3.3 V-> 2.5 V -> 1.3 V. The –64V and –32V rails will come up after the +12 V rail. The only power sequencing requirement on the board comes from the IXP425 Network Processor, which requires that +3.3 V comes up before or at the same time as +1.3 V. JP9 is provided for +3V3 (+3.3 V) measurement vs. +3V3_CJ.

The +1V3 (+1.3 V) rail required by the IXP425 Network Processor is implemented directly onto BIXMB425BD base card (Sheet 28 - +1V3 Regulator for the IXP425 Network Processor core). +1V3 (+1.3 V) is generated from +3V3 (+3.3 V) using the National Semiconductor LP3965ES-ADJ voltage regulator. JP13 is placed for +1V3 measuring purposes.

Ground headers (JP5, JP2, JP4, JP7, JP1, JP10) are provided and they are located distributed on the board to provide easy ground points access.

There is a gasp circuit designed to monitor the +12V and +5V to indicate early warning of power failure to the UTOPIA2 connector (GASP_INT_N).

The standard power card that is shipped with the board supplies a power of 50 W, and is capable of supporting a standard configuration on the IXP425 Network Processor.

Table 32. Power Connector J7 (Sheet 1 of 2)

Row A Pin #	Signal	Row B Pin #	Signal
1	-64V	2	-32V
3	GND	4	GND
5	GND	6	GND
7	+2V5	8	GND
9	+2V5	10	+3V3
11	GND	12	+3V3
13	GND	14	+3V3

Table 32. Power Connector J7 (Sheet 2 of 2)

Row A Pin #	Signal	Row B Pin #	Signal
15	GND	16	+3V3
17	GND	18	+3V3
19	GND	20	GND
21	+5V	22	GND
23	+5V	24	EN_3V3
25	+5V	26	+5V
27	GND	28	+12V
29	GND	30	+12V

3.15 Reset Logic

The system reset is generated with two polarities, RST_N, RST, for several cases on the IXP425 Network Processor (Sheet 27 – Reset Circuit). The IXP425 Network Processor is reset whenever a system reset, RST_N, is asserted. This action is done when the following occur:

- Power rails are not at appropriate levels at the LTC1728ES5-2.5 Supply Monitor. The LTC1728 has an open drain output. Reset asserted for a minimum of 140ms when:
  +3V3 (+3.3 V) rail < +3.086 V
  +2V5 (+2.5 V) rail < +2.338 V
  +1V3 (+1.3 V) rail < +1.182 V
  In the above case, PWRON_RST_N is asserted as well.
- Reset button on the BIXMB425BD base board has been pressed (SW1 Push Button)
- System reset generated out of JTAG circuitry (ICE or boundary scan), JTG_SRST_N

3.15.1 Design Notes

RST_N of MAX6355 and RST_N of LTC1728ES5 are open drain outputs, so pull-ups are necessary.

3.16 Clocking

There are several oscillators socketed on the BIXMB425BD base card to allow clocking requirement flexibility when prototyping a design. The following the IXP425 Network Processor interfaces require oscillators on the BIXMB425BD base board.

- IXP425 Network Processor system clock – 33.33 MHz (Sheet 3)
- UTOPIA-2 input and output clock – 33 MHz (may be disabled through jumper, JP12 option) (Sheet 9)
- PCI host clock – 33 MHz and 66 MHz (Header, J11 option) (Sheet 26)
- Expansion bus clock – 33 MHz external oscillator or GPIO15 selectable (jumper, JP6 option) (Sheet 26)

The expansion bus and PCI will share the 33MHz oscillator. Although UTOPIA-2 also require a 33 MHz oscillators, a separate oscillator is used and implemented on the BIXMB425BD base card to allow the oscillator frequency to be altered or disabled independently (Sheet 9)

The PCI_CLK_TO_CJ / PCI_CLKIN is driven by either the IXP425 Network Processor GPIO14 / PCI_CLK_FROM_CJ or an external oscillator when the IXP425 Network Processor is PCI host. A jumper option, J11 is provided to select between the IXP425 Network Processor clock, 33 MHz external oscillator, and 66 MHz external oscillator. The clock is driven through a clock driver.

The expansion bus clock is driven through GPIO15 / EXPB_CLK_TO_CJ or using an on board oscillator. A jumper option, JP6 determines the clock source. The clock, EXPB_CLK_TO_CJ, is driven out of a clock driver to ensure proper signal strength at the multiple endpoints.

The HSS clocks (HSS_TXCLK0, HSS_RXCLK0, HSS_TXCLK1, HSS_RXCLK1) can be sourced from the IXP425 Network Processor. The clock source is software configurable within the IXP425 Network Processor. Although this capability is present, the IXP425 Network Processor defaults to an external HSS clock source, i.e., HSS_TXCLK0, HSS_RXCLK0, HSS_TXCLK1, HSS_RXCLK1 are all input pins. In this case, HSS-0 and HSS-1 cards are required to have on board oscillators to clock the HSS interface.

The ENET clocks (ETH_TXCLK0, ETH_RXCLK0, ETH_TXCLK1, ETH_RXCLK1) are sourced from the ENET-0 and ENET-1 cards. This implies that on board oscillators are required on the ENET-0 and ENET-1 cards.

3.17 Mechanical Dimensions

With all cards plugged onto BIXMB425BD base card, the dimensions of platform is 9”x11.” The base card have devices populated on both sides of the board.

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BIXD100, BIXD110, BIXD120 Cards Hardware Design Description 4

The BIXD100 Ethernet PHY Card, BIXD110 ADSL Card and BIXD120 Voltage Regulator Card are all built compatible to the connectors available on the BIXMB425BD base card.

4.1 BIXD100 Ethernet PHY Card

4.1.1 Introduction

The BIXD100 Ethernet Cards are compatible to ENET-0 or ENET-1 connectors on BIXMB425BD base card. The BIXD100 Ethernet Card plugs into ENET-0 or ENET-1 connector on BIXMB425BD base card through the 2x60 pin J1 connector. See Section 3.7.3 for a description of these connectors on the BIXMB425BD base card. The two BIXD100 cards use the Intel LXT972A. The Intel LXT972A is a dual-speed, full-duplex 10/100 Fast Ethernet transceiver (PHY). It provides Media Independent Interface (MII) for attachment to one of the two 10/100 Media Access Controller (MAC) within the IXP425 Network Processor. The reference of BIXD100 in this platform design will be known as ENET-0 and ENET-1.

More information about the LXT972A can be found in the *Intel®LXT972A 3.3V Dual-Speed Fast Ethernet Transceiver Datasheet*.

Each BIXD100 card map its own address to the IXP425 Network Processor's memory map. JP2 defines the address of BIXD100. The setting on this jumper must be different if two BIXMB425BD Ethernet PHY cards are plugged into BIXMB425BD base card. For ENET-0, JP2 pin 1 and 2 must be shunted. For ENET-1, JP2 pin 2 and 3 must be shunted.

The LXT972A clock (REFCLK-X1) on each BIXD100 Ethernet Card are clocked using an on board (on the BIXD100) 25-MHz oscillator. A 25-MHz crystal can be used if desired but this is not populated on BIXD100. The LXT972A TX_CLK and RX_CLK will supply transmit and receive clocks to the IXP425 Network Processor via the connector (ENET_TX_CLK, ENET_RX_CLK) (Sheet 4 BIXD100 Schematics).

There are three LEDs (DL1) located at the sides of the BIXD100 Ethernet PHY Card. They indicated 10/100 mode, link and activity status.

JP1, JP3, JP4 are provided and distributed on the BIXD100 card to access to the GND plane.

+3V3_ENET analog power is generated on the BIXD100 Ethernet Card from the +3V3 (+3.3V) power delivered to it by the BIXMB425BD base card. This is needed by LXT972A and the transformer.

Figure 7. BIXD100 Ethernet Card Block Diagram

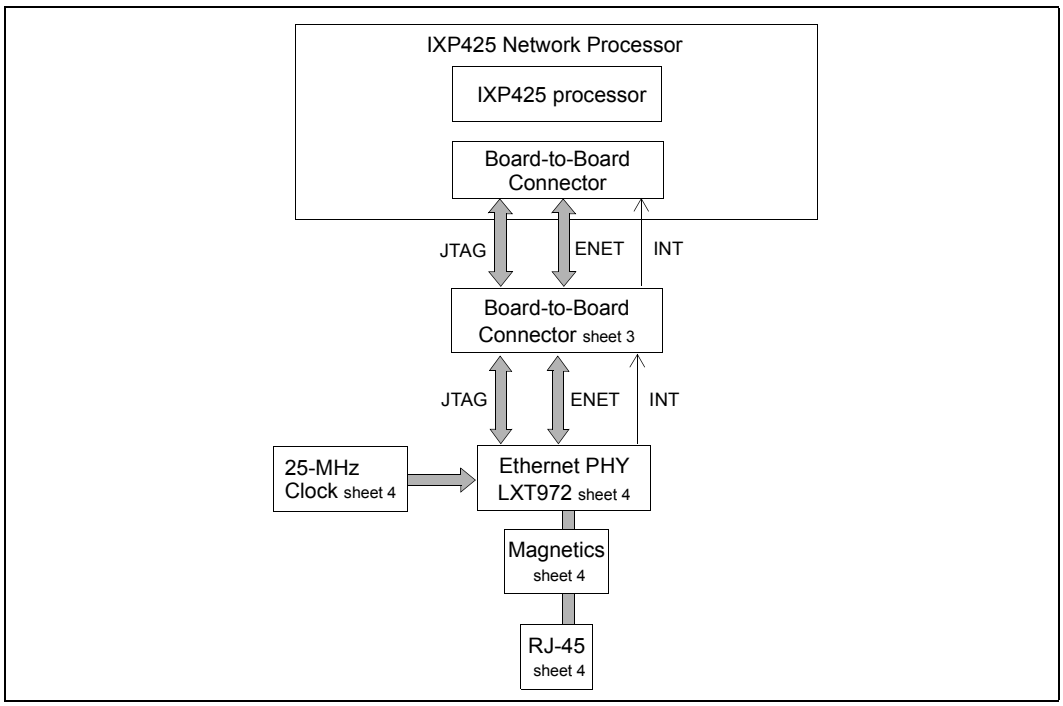
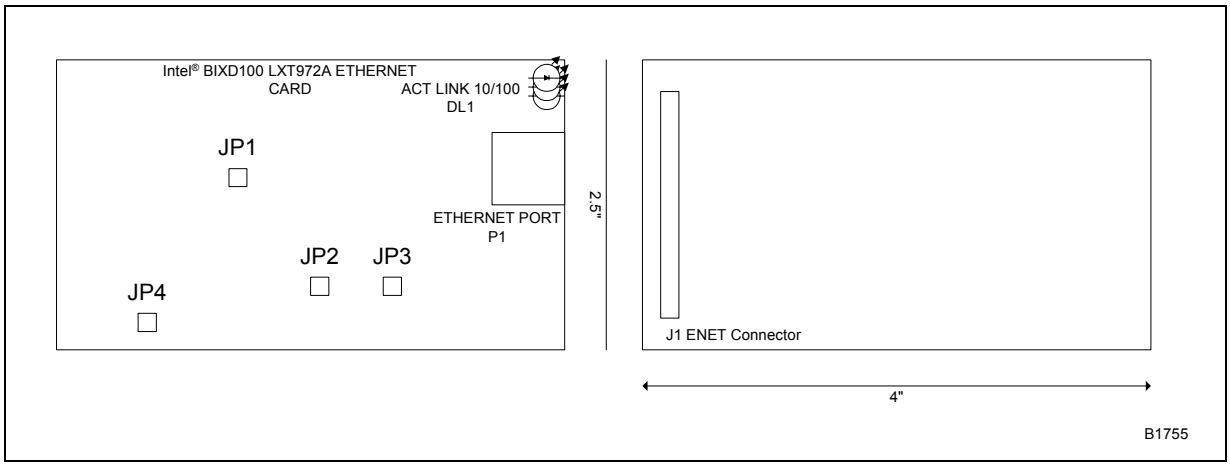


Figure 8. BIXD100 Ethernet Card Component Placement Diagram



4.1.2 BIXD100 Ethernet Card Signals

The BIXD100 Ethernet Card plugs into ENET-0 or ENET-1 using a 2x60 pin connector (J1) on the BIXD100 that is compatible with either ENET-0 (J13) or ENET-1 (J6) connector on the BIXMB425BD Base card. The BIXD100 connector (Sheet 3 of BIXD100 Schematics) has on board card signals used by devices (LXT972A, oscillator, LEDs) on the BIXD100 Ethernet Card routed to it. These signals include the following:

- Power/Ground
- JTAG Signals
- MII Signals
- Other Connector Signals
- Expansion bus, GPIO and Expansion bus clock signals on ENET-0 and ENET-1 connectors on BIXMB425BD base card are not used on BIXD100. Therefore these signals are not routed to the BIXD100 connector and does not exist on BIXD100.

The signals that exist on BIXD100 Ethernet Card are categorized in Table 33.

Table 33. Signals on BIXD100 Ethernet Card (Sheet 1 of 3)

Signals on BIXD100	Type I/O		Intel® LXT-972A (single port)
Power/Ground			
-64V	PWR		Not Used
-32V	PWR		Not Used
+12V	PWR		Not Used
+5V	PWR		Not Used
+3V3	PWR		~125mA 300mW
+3V3_ENET	PWR (Analog)		VCCA0, VCCA1, Transformer
+2V5	PWR		No
GND	GND		GND
Expansion Bus Signals			
EXPB_ADDR[23:0]	I		Not Used
EXPB_D[15:0]	I/O		Not Used
EXPB_WR_N	I		Not Used
EXPB_HRDY_N0	I		Not Used
EXPB_RD_N	I		Not Used
EXPB_CLK	I		Not Used
EXPB_ALE	I		Not Used
ENET_INT_N / unpopulated Pull up resistor	O (OD)		ENET_INT_N (MDINT_N)
EXPB_CS_N	I		Not Used
EXPB_IOWAIT_N	O		Not Used

Table 33. Signals on BIXD100 Ethernet Card (Sheet 2 of 3)

Signals on BIXD100	Type I/O		Intel® LXT-972A (single port)
JTAG Signals			
JTAG_TDI	I		TDI
JTAG_TDO	O		TDO
JTAG_TMS	I		TMS
JTAG_TCK	I		TCK
MII Signals			
ENET_RXD[3:0]	O		RXD[3:0]
ENET_RX_DV	O		RX_DV
ENET_RX_CLK	O		RX_CLK
ENET_RX_ER	O		Test Point
ENET_RX_EN	I		Not Used
ENET_TX_CLK	O		TX_CLK
ENET_TX_EN	I		TX_EN
ENET_TX_ER	I		TX_ER (pulled low)
ENET_TXD[3:0]	I		TXD[3:0]
ENET_COL	O		COL
ENET_CRS	O		CRS
Other Connector Signals			
RST_N	I		RESET_N
ENET_MDIO	I/O		MDIO
ENET_MDC	I		MDC
ENET_PWRDWN	I		PWRDWN (pulled down)
LXT972A Specific Signals			
MDDIS pulled down	I		MDDIS
25MHz Oscillator	I		REFCLK-XI (25MHz)
25MHz Crystal (Do Not Populate)	O		XO
ENET_INT_N	O.D.		MD_INT_N
JP2 (option to pull up or pull down)	I		ADDR0
TXSLEW0 (pulled high)	I		TXSLEW0
TXSLEW1 (pulled low)	I		TXSLEW1
RBIAS (pulled down)	Analog I		RBIAS
PAUSE (pulled high)	I		PAUSE
TEST[1:0] (pulled down)	I		TEST[1:0]

Table 33. Signals on BIXD100 Ethernet Card (Sheet 3 of 3)

Signals on BIXD100	Type I/O		Intel® LXT-972A (single port)
LEDs			
LED/CFG3	I/O		LED-CFG3
LED/CFG2	I/O		LED-CFG2
LED/CFG1	I/O		LED-CFG1
RJ-45 Port Signals			
TPFOP	O		TPFOP
TPFON	O		TPFON
TPFIP	I		TPFIP
TPFIN	I		TPFIN

4.2 BIXD110 ADSL Card Definition

The BIXD110 ADSL card for BIXMB425BD base card uses the Alcatel* MTK-20150 Chipset that consists of the Alcatel MTC-20156 and Alcatel MTC-20154. The MTC-20156 is the DMT modem, ATM Framer, and controller chip of the chipset. The MTC-20154 is the supporting Analog Front End. The 2x60 pin J3 connector available on the BIXD110 ADSL card will plug into the 2x60 pin Utopia 2 connector on the BIXMB425BD base card. See Section 3.7.1 for a description of this Utopia connector on the BIXMB425BD base card.

The BIXD110 ADSL card design will support multiple channels through the single channel Alcatel MTK-20150 chipset using a stackable design.

+12 V, +5 V, +3V3 (+3.3 V) and +2V5 (+2.5 V) digital voltage rails are provided from BIXMB425BD base card to the Utopia-2 Connector. Other voltages, both digital and analog, required for the card is derived from these voltages on the BIXD110 ADSL Card. The –12V voltage rail is derived from the +3V3 (+3.3V) voltage rail on the card. JP4, JP5, JP6 headers provide access to GND plane.

The majority of the signals needed to support the DSL card are Expansion Bus and Utopia 2 data interface signals. The Alcatel DMT on the ADSL card will receive its UTP_RX_CLK and UTP_TX_CLK through the 33 MHz oscillator already implemented on the BIXMB425BD base card. The same oscillator on the base card is used to provide UTP_OP_CLK and UTP_IP_CLK signals to the IXP425 Network Processor. (Sheet 9 – BIXMB425BD Base Card Schematics).

Figure 9. BIXD110 ADSL Card Block Diagram

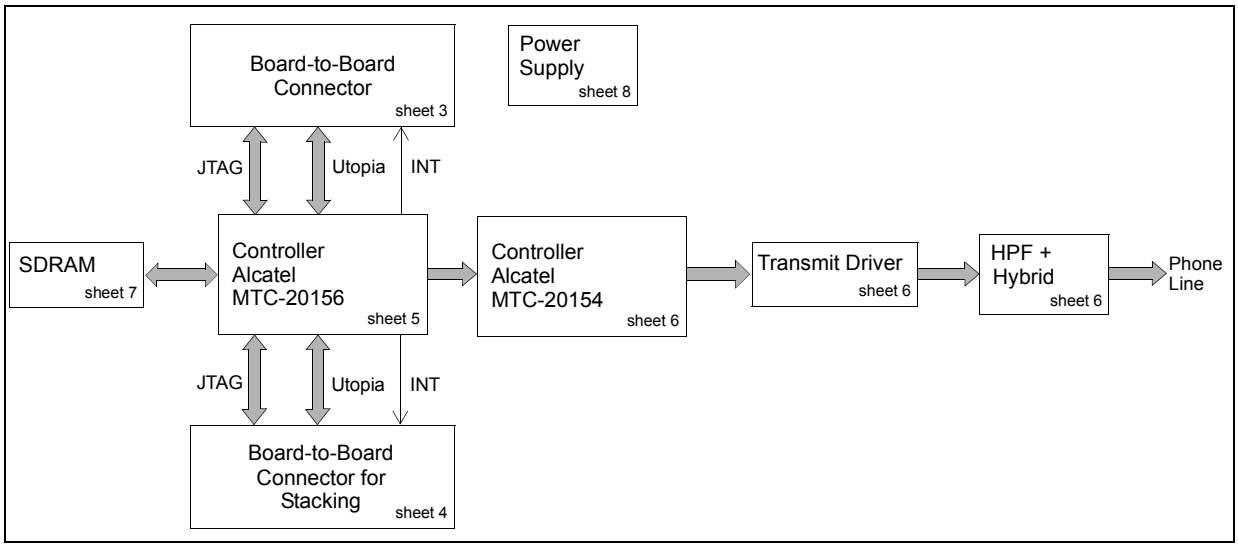
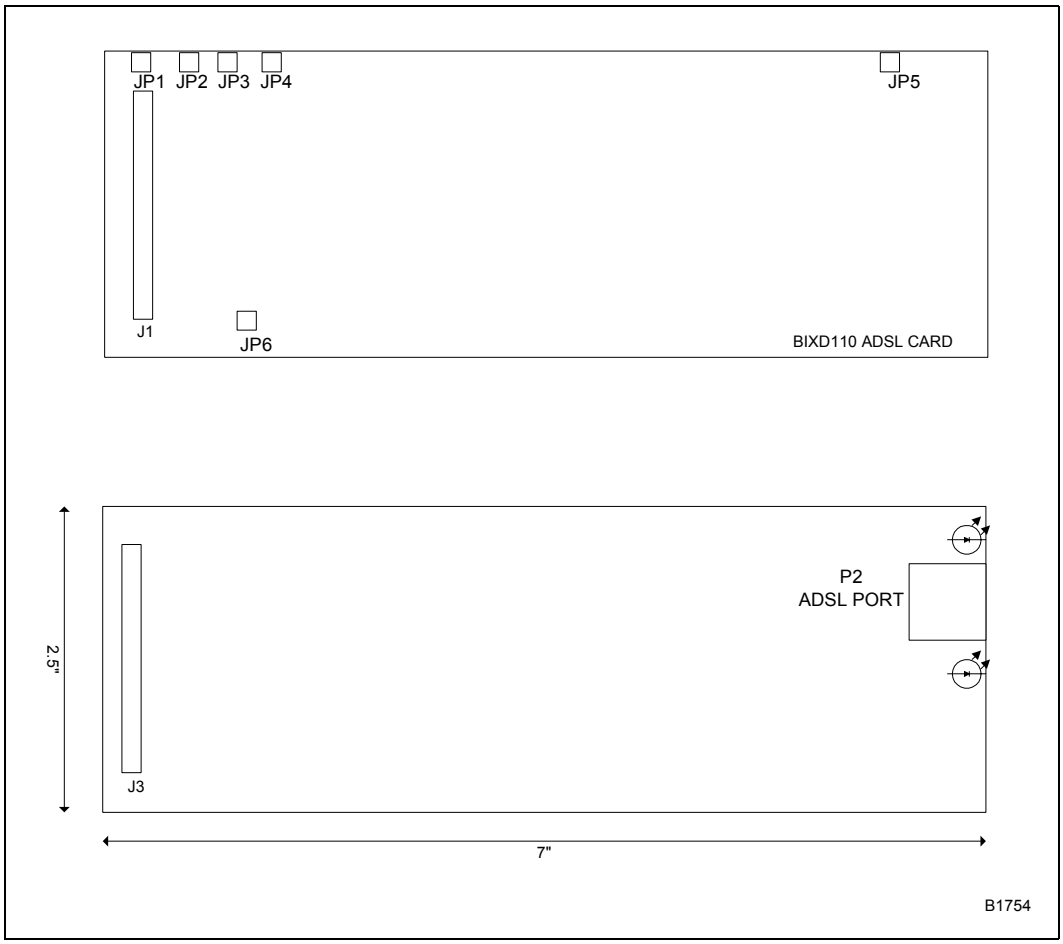
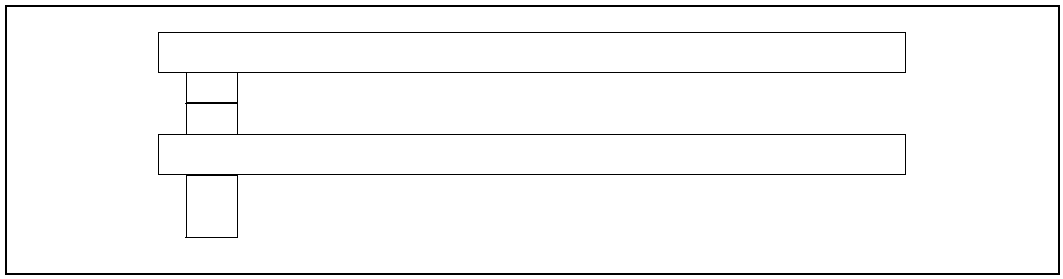


Figure 10. BIXD110 ADSL Card Component Placement Diagram



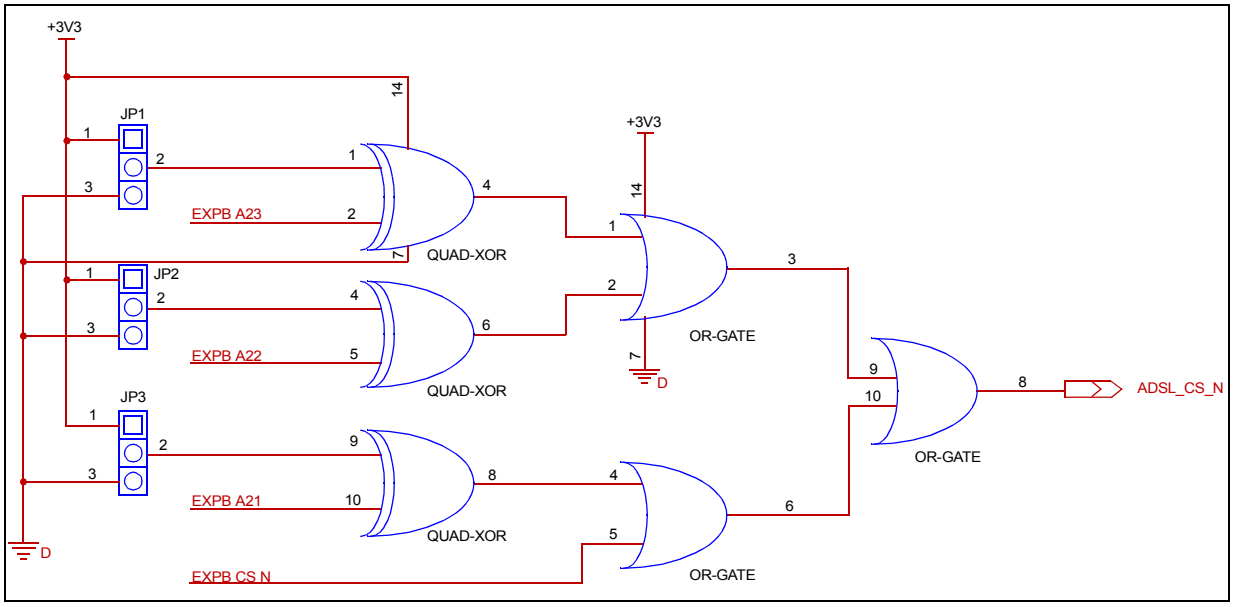
To have multi-channel PHY support, multiple BIXD110 ADSL cards can be stacked on top of each other through the board to board stacking connector.

Figure 11. Side View of 2-Stacked Cards



The card will have a plug connector on the bottom side and a receptacle connector on the top side to allow them to stack as seen in Figure 11.

Figure 12. ADSL Stacking Logic



Each card has its own address space. Each card has three 3-pin jumpers that allow the user to define the address space for that particular card (JP3, JP2, JP1). (See Sheet 3 BIXD110 ADSL Card schematics) A single expansion bus chip select along with the expansion bus addresses defined on each card allows individual communication to each device. Figure above shows the ADSL Stacking Logic. The top three expansion bus address lines are compared to the address set on the jumpers. If the address matches and an expansion bus chip select has been asserted, then the expansion bus chip select will drive that particular card. The interrupt on each card is open-drain to allow sharing of the interrupt sent to the IXP425 Network Processor.

4.2.1 BIXD110 ADSL Card Signals Description

The BIXD110 ADSL Card plugs into the UTOPIA-2 connector on the BIXMB425BD base card using a 2x60 pin connector on the BIXD110. This connector is compatible with Utopia 2 connector on the BIXMB425BD Base card. The BIXD110 connector (See Sheet 3 of BIXD110 Schematics) has on board card signals used by devices (MTC-20156 DMT, MTC-20154 AFE, transmit driver, LEDs) on the BIXD110 ADSL Card routed to it. These signals include the following:

- Power/Ground
- Utopia Signals
- Other Connector Signals
- JTAG Signals
- Expansion bus Signals

The signals that exist on BIXD110 ADSL Card are categorized in Table 34.

Table 34. BIXD110 ADSL Card Signals (Sheet 1 of 4)

Signals on BIXD110 ADSL Card	Type I/O	On Connector	Alcatel ADSL Annex A
Power/Ground			
+12V	PWR	+12VIN	
CPE_DRV_12VPOS (derived from +12V)	PWR (Analog)	Not available	+V1, +V2 (AD8016ARB)
CPE_DRV_12VNEG (Derived from -12V)	PWR (Analog)	Not available	-V1, -V2 (AD8016ARB)
-12V (derived from +3V3)	PWR	Not available	Not Used
+5V	PWR	+5V	Not Used
+3V3	PWR	+3V3	Not Used
20156_3V3, 20154_A23V3, 20154_D3V3	PWR (Analog)	Not available	VDDIO[15:0] (MTC20156), DVDD[1:0] (MTC20154)
+2V5	PWR	+2V5	Not Used
GND	GND	GND	GND
GND	GND (Analog)	GND	GND

Table 34. BIXD110 ADSL Card Signals (Sheet 2 of 4)

Signals on BIXD110 ADSL Card	Type I/O	On Connector	Alcatel ADSL Annex A
UTOPIA Signals			
UTP_RX_ADDR[4:0]	I/O	UTP_RX_ADDR[4:0]	U_RXADDR[4:0]
UTP_RX_DATA[7:0]	I/O	UTP_RX_DATA[7:0]	U_RXDATA[7:0]
UTP_RX_SOC	I	UTP_RX_SOC	U_RXSOC
UTP_RX_EN_N	I	UTP_RX_EN_N	U_RXENB_N
UTP_RX_CLAV	O	UTP_RX_CLAV	U_RXCLAV
UTP_RX_CLK	I	UTP_RX_CLK	U_RXCLK
UTP_TX_ADDR[4:0]	I/O	UTP_TX_ADDR[4:0]	U_TXADDR[4:0]
UTP_TX_DATA[7:0]	I	UTP_TX_DATA[7:0]	U_TXDATA[7:0]
UTP_TX_SOC	I	UTP_TX_SOC	U_TXSOC
UTP_TX_EN_N	I	UTP_TX_EN_N	U_TXENB_N
UTP_TX_CLAV	O	UTP_TX_CLAV	U_TXCLAV
UTP_TX_CLK	I	UTP_TX_CLK	U_TXCLK
ADSL_RDY_N	O (OD)	ADSL_RDY_N (EX_CS_N1)	C_RDY_N
JTAG Signals			
JTAG_TDI	I	JTAG_TDI	TDI
JTAG_TDO	O	JTAG_TDO	TDO
JTAG_TMS	I	JTAG_TMS	TMS
JTAG_TCK	I	JTAG_TCK	TCK

Table 34. BIXD110 ADSL Card Signals (Sheet 3 of 4)

Signals on BIXD110 ADSL Card	Type I/O	On Connector	Alcatel ADSL Annex A
Expansion Bus Signals			
EXPB_A[9:0]	I	EXPB_A[9:0]	CA[8:0]
EXPB_D[7:0]	O	EXPB_D[7:0]	CD[7:0]
ADSL_CS_N	I	DSL_CS_N	C_CS_N
EXPB_CLK	I	EXPB_CLK	Not Used
EXPB_WR_N	I	ADSL_WR_N	C_WR_N
EXPB_RD_N	I	ADSL_RD_N	C_RD_N
EXPB_ALE	I	EXPB_ALE	Not Used
Other Connector Signals			
ADSL_RST_N	I	ADSL_RST_N	CARM_RESET_N and SACHEM_RESET_N
ADSL_INT_N	O (OD)	ADSL_INT_N	C_INT_N
ADSL_GASP_INT	I	ADSL_GASP_INT	IDDQ
On-Card Signals			
AFE_TX[3:0]	O	Not Used	AFTXD[3:0]
AFE_RX[3:0]	I	Not Used	AFRXD[3:0]
AFE_CLKWD	I	Not Used	CLWD
AFE_PWD	O	Not Used	POWER_LOW_N
AFE_CTRLIN	I	Not Used	CTRLDATA
UTP_RX_REFB (No connect)	I	Not Used	UTP_RXREFB
UTP_TX_REFB to 20156_3V3	I/O	Not Used	UTP_TXREFB
AFE_MCLK	I	Not Used	MCLK
MODE[1:0] pull down	I/O	Not Used	MODE[1:0]
C_MODE[1:0]	I/O	Not Used	C_MODE[1:0]
ADSL_TX	I/O	Not Used	RSTXD1
ADSL_RX	I/O	Not Used	RSRXD1
PA[1:0] to LEDs	O	Not Used	PA[1:0]
PA14	I/O	Not Used	PA14
PA15	I/O	Not Used	PA15
TROM	I	Not Used	TROM
T_ACK	O	Not Used	T_ACK
T_REQA	I	Not Used	T_REQA
T_REQB	I	Not Used	T_REQB
TESTSE	I	Not Used	TESTSE
SCAN_CLK	I	Not Used	SCAN_CLK
GP	I	Not Used	GP

Table 34. BIXD110 ADSL Card Signals (Sheet 4 of 4)

Signals on BIXD110 ADSL Card	Type I/O	On Connector	Alcatel ADSL Annex A
Memory Signals			
ADSL_SDRAM_ADDR[15:0]	O	Not Used	EA[15:0]
ADSL_SDRAM_DATA[15:0]	I/O	Not Used	ED[15:0]
ADSL_SDRAM_CS_N	O	Not Used	S_CS_N
ADSL_SDRAM_CLK	O	Not Used	E_CLK
ADSL_SDRAM_RAS_N	O	Not Used	S_RAS_N
ADSL_SDRAM_CAS_N	O	Not Used	S_CAS_N
ADSL_SDRAM_UDQM_N	O	Not Used	S_nUDQM
ADSL_SDRAM_ULDQM_N	O	Not Used	S_nLDQM
ADSL_SDRAM_CS0_N (No Connect)	O	Not Used	CS0_N
ADSL_SDRAM_OE_N (No Connect)	O	Not Used	S_OE_N

4.3 BIXD120 Voltage Regulator Card

4.3.1 Introduction

BIXMB425BD base card receives its power through the BIXD120 voltage regulator card. The BIXD120 voltage regulator card is plugged into the BIXMB425BD base card through the 30-pin connector on the base card. See Section 3.14 for a description of this connector on the BIXMB425BD base card. The BIXD120 power card provides +12V, +5V, +3V3 (+3.3V), +2V5 (+2.5 V), -64 V, and –32 V to the BIXMB425BD Development platform base card. The power card generates voltages on the board from power supplied through a single power brick connection. Power on the BIXD120 voltage regulator card is supplied through a single 5pin DIN male connector from an external power supply to a female connector placed on the card. This power brick will provide +12 V at 2A, +5 V at 5A to the BIXD120 card. +3V3 (+3.3 V) at 7A, +2V5 (+2.5 V) at 1.5A, -64 V at 0.3A, and –32 V at 0.6A are generated on the BIXD120 Voltage regulator Card.

The ENABLE_3V3 enables BIXMB425BD base card to control +3V3 (+3.3 V) voltage regulation.

The power-up sequence requirements are: 12 V ->5 V ->3.3 V->2.5 V. The –32 V and –64 V rails have no sequencing requirement, but will rise after the 12V rail. Power-down will occur in the opposite order. The BIXD120 handles this power sequence requirements for the BIXMB425BD base card and the IXP425 Network Processor. Power measurement capability is also provided through jumpers on the BIXD120.

JP2, JP3 are provided for measurement purposes for -32V and -64V. If the BIXD120 Voltage Regulator Card is not connected to BIXMB425BD Base Card, JP1 must be shunted.

DL1 (+12V), DL3 (+5V), DL4(+3.3V), DL2(+2.5V) will light up in red color once the voltages are regulated.

Figure 13. BIXD120 Voltage Regulator Card Block Diagram

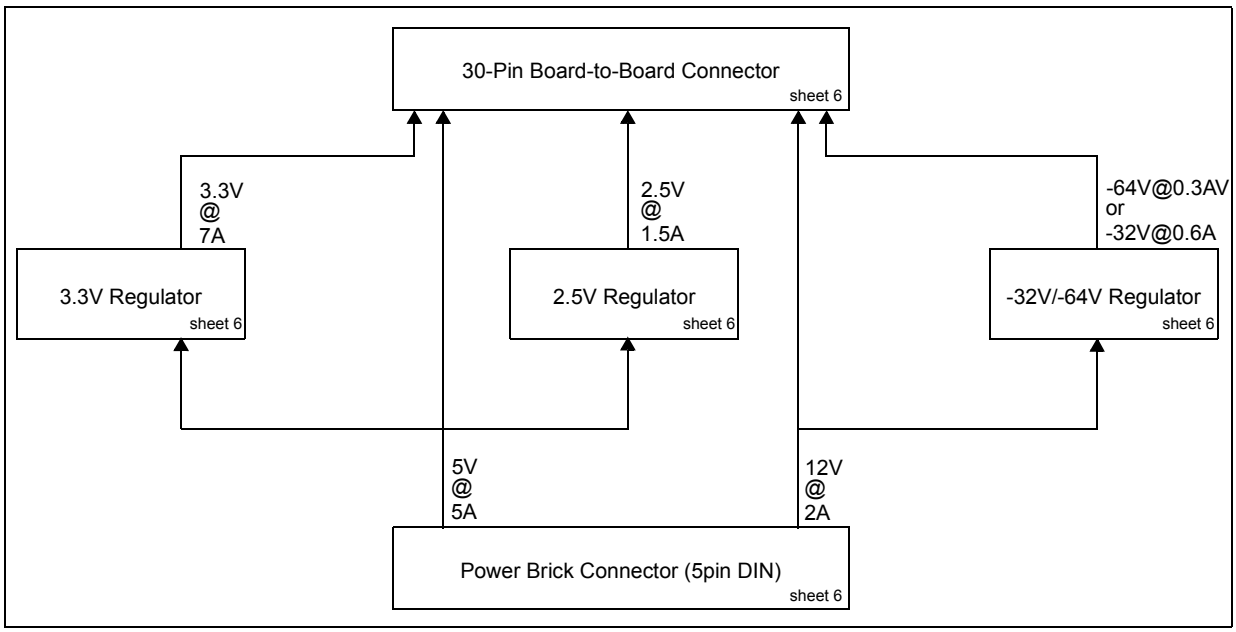
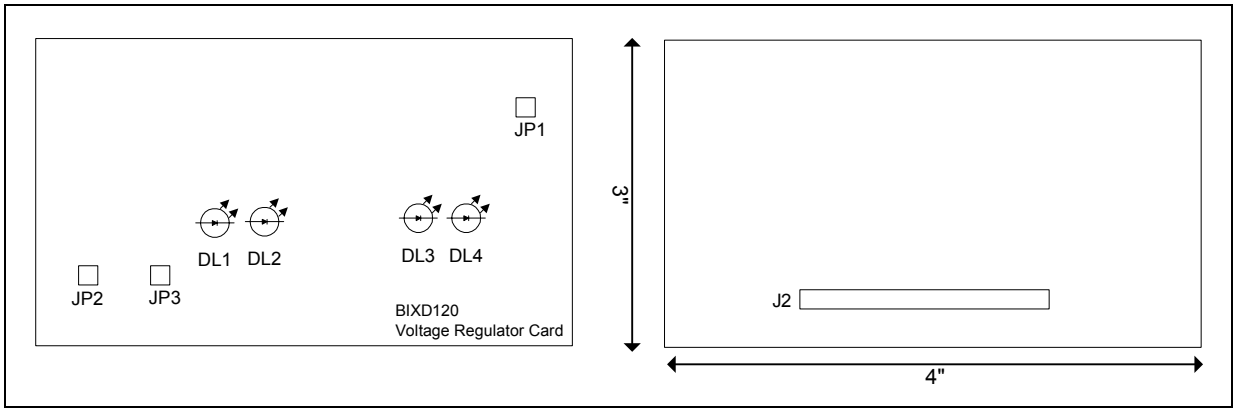


Figure 14. BIXD120 Voltage Regulator Card Component Placement Diagram



4.3.2 BIXD120 Voltage Regulator Card Signals Description

Table 35. Power Connector J2 Pinout

Row A Pin #	Signal	Row B Pin #	Signal
1	-64V	2	-32V
3	GND	4	GND
5	GND	6	GND
7	+2V5	8	GND
9	+2V5	10	+3V3
11	GND	12	+3V3
13	GND	14	+3V3
15	GND	16	+3V3
17	GND	18	+3V3
19	GND	20	GND
21	GND	22	GND
23	+12V	24	ENABLE_3V3
25	+12V	26	+5V
27	GND	28	+5V
29	GND	30	+5V

Power is supplied to the BIXMB425BD base card through a 2x15-pin board to board J2 connector, shown in table above. The connector was developed based on the estimates for the worst case platform power requirements and the worst-case current-handling capability of 3 mA/pin for the components that are used. The 30-pin connector used on the card is the Samtec* IPS1-115-01-S-D-POL. It is a 30-pin plug through-hole connector with 0.1 inch center. The mating connector on the base card is the Samtec IPT1-115-01-S-D-POL receptacle.

4.3.3 Regulators

The regulators chosen for the card design are listed in Table 36.

Table 36. Regulator Details (Sheet 1 of 2)

Output voltage	3.3V	2.5V	-64V/-32V
Vendor	Maxim	Maxim	Linear Tech
Part number	MAX767	MAX1644	LT1619
Output power	23.1W	3.75W	20W total
Output current	7A	1.5A	0.3A@-65V or 0.6A@-32.5V
Input voltage	5V	5V	12V
Conversion type	Buck	Buck	Flyback
Efficiency	>90%	>80%	>50%
Transient response	~100mV	<100mV	Not documented

Table 36. Regulator Details (Sheet 2 of 2)

Output voltage	3.3V	2.5V	-64V/-32V
Reference design available	Yes	Yes	Yes
Maximum efficiency losses	2W	1W	3.5W
Maximum ripple	±20mV	±40mV	Not documented
Minimum load current	1.5mA	1mA	Not documented

Some observations of the regulators chosen are:

- The MAX767 will remove the drive voltage to the high side MOSFET whenever the voltage across the sense resistor is above 100mV in order to protect the circuit during a short circuit condition.
- The MAX1644 can withstand continuous high current and has a thermal shutdown feature.
- The LT1619 is assumed to not have overpower protection. The efficiency for the LT1619 is low at low output currents, but it rises significantly as output current increases.

Layout Guidelines A

A.1 General Guidelines

- # Layers = Based on layout designer's recommendations
- Line / Space: 5 mil / 5 mil minimum
- Via size: 12 drill / 24 pad
- Target impedance 65 Ω on all signal layers
- Gold finish (to accommodate BGA socket)
- 100% net coverage for flying probe test. Preferably on bottom side.
- Test points called out in the schematics should be same size as test points for flying probe.
- Group decoupling caps as shown on schematics (next to associated logic).
- Oscillators: Place within 1" of logic device.
- Do not route high-speed signals (PCI*, EXPB*, UTP*, SDM*, *CLK*) across power plane splits.

BIXMB425BD Base Card must fit into a 6U compactPCI chassis. Therefore, the width must be 233.35 mm. The length may be extended beyond the standard 160 mm.

A.2 Card Mounting Holes

- All mounting holes must be:
  - 0.125" finished inner diameter
  - 0.160" pad
- Place one mounting hole in each corner.
- Mounting holes should be grounded to all GND_DIGITAL planes.

If dimension (x or y) spans greater than 4", place an additional mounting hole mid-way along the outer edge of the card.

A.3 Clocks

- Trace length of UTP_IP_CLK from R54 to J3 should be equal the length between R54 and U1 (within ½ inch).
- Trace length of UTP_OP_CLK from R55 to J3 should be equal the length between R55 and U1 (within ½ inch).
- Trace lengths of all clock signals leaving U29 (EXPB_CLK_TO_CJ, EXPB_CLK_ENET0, EXPB_CLK, ENET1, EXPB_CLK_UTP, EXPB_CLK_HSSW, EXPB_CLK_HSSV) should be matched (within ½ inch).
- Trace lengths of all clock signals leaving U30 (PCI_CLK_S0, PCI_CLK_S1, PCI_CLK_S2, PCI_CLK_S3, PCI_CLK_TO_CJ) should be matched (within ½ inch).
- Y3 and Y4 should be placed within 1 inch of U29 and U30.

A.4 JTAG

- The JTAG boundary scan port (J14) and ICE JTAG port (J16) should be placed next to each other in order to minimize stubs.
- U38, U39 should be placed near to J14 and J16.
- The following traces should have the same length (L):

CUDJ_TDI	JTAG_TDO + COR_TDO
CUDJ_TDO	JTAG_TDO+ICE_TDO
ENET0_TDI	TMS_S0 + CUDJ_TMS
ENET0_TDO	TMS_S1 + ENET0_TMS
ENET1_TDI	TMS_S2 + ENET1_TMS
ENET1_TDO	TMS_S3 + DSL_TMS
DSL_TDI	TMS_S4 + VOICE_TMS
DSL_TDO	TMS_S5 + HSSW_TMS
PCI0_TDI	TMS_S6 + PCI0_TMS
PCI0_TDO	TMS_S7 + PCI1_TMS
PCI1_TDI	TMS_S8 + PCI2_TMS
PCI1_TDO	TMS_S9 + PCI3_TMS
PCI2_TDI	TMS_S9 + CPCI_TMS
PCI2_TDO	TCK_S0 + CUDJ_TCK
PCI3_TDI	TCK_S1 + ENET0_TCK
PCI3_TDO	TCK_S2 + ENET1_TCK
HSSW_TDI	TCK_S3 + DSL_TCK
HSSW_TDO	TCK_S4 + VOICE_TCK

VOICE_TDI	TCK_S5 + HSSW_TCK
VOICE_TDO	TCK_S6 + PCI0_TCK
CPCI_TDI	TCK_S7 + PCI1_TCK
CPCI_TDO	TCK_S8 + PCI2_TCK
JTAG_TDI + COR_TDI	TMS_S9 + PCI3_TCK
JTAG_TDI+ICE_TDI	TMS_S9 + CPCI_TCK

A.5 PCI

- Series resistors near compactPCI slot (J10) must be placed within 15.2 mm of the signal's connector pin.
- Trace length of all PCI signals between compactPCI connector (J10) and the IXP425 Network Processor (U1) must be less than or equal to 63.5 mm. This includes the length between the series resistor and the connector.
- Characteristic impedance on compactPCI signal traces must be 65 Ω plus or minus 10%.
- PCI clock (CPCI_CLK_TO_CJ + J1CK + PCI_CLK_TO_CJ) trace length must be 63.5 mm plus or minus 2.54 mm between the compact PCI connector and the IXP425 Network Processor.
- The resistors on Sheet 18 of the BIXMB425BD schematics (R136-R230) should share a pad when the same net goes to two pads.

A.6 USB

USB_D+ and USB_D- trace lengths should be matched and routed at 90 Ω differential.

A.7 Power

- Power is distributed through J12. Each pin on J12 can handle up to 7 A of current. Layout should be designed to also handle up to 7 A from each pin.
- U33 and associated components should be placed near J12 (within 1 inch).
- R405, R406, and C246 should be placed as close as possible to U37. Other components related to U37 should also be placed nearby.

A.8 LEDs and displays

- LEDs DL1-6 should be placed adjacent to each other. The order should be (left to right): DL2, DL3, DL4, DL5, DL6, and DL1.
- Hexadecimal displays U10-U13 should be placed in the order (left to right) U10, U11, U12, and U13.

- Dual-color LEDs DL7-DL22 should be placed in the order: DL22, DL21, DL20, DL19, DL18, DL17, DL16, DL15, DL14, DL13, DL12, DL11, DL10, DL9, DL8, and DL7.

A.9 Switches

- Place SPDT dip switches in the order: SW7, SW5, SW3, and SW1.
- Place SPST dip switches in the order: SW6, SW4, and SW2.